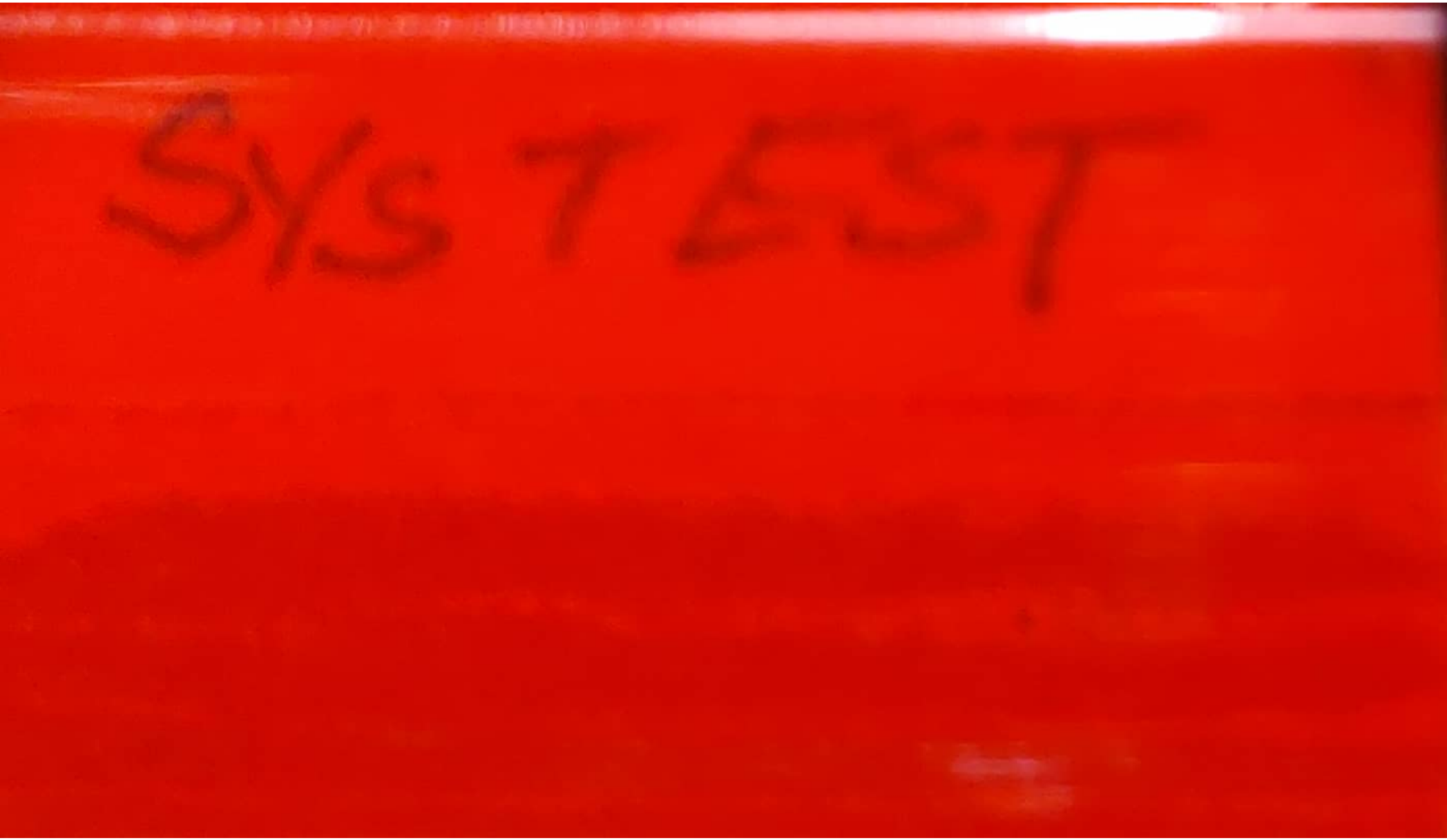
Mine Collins Tester

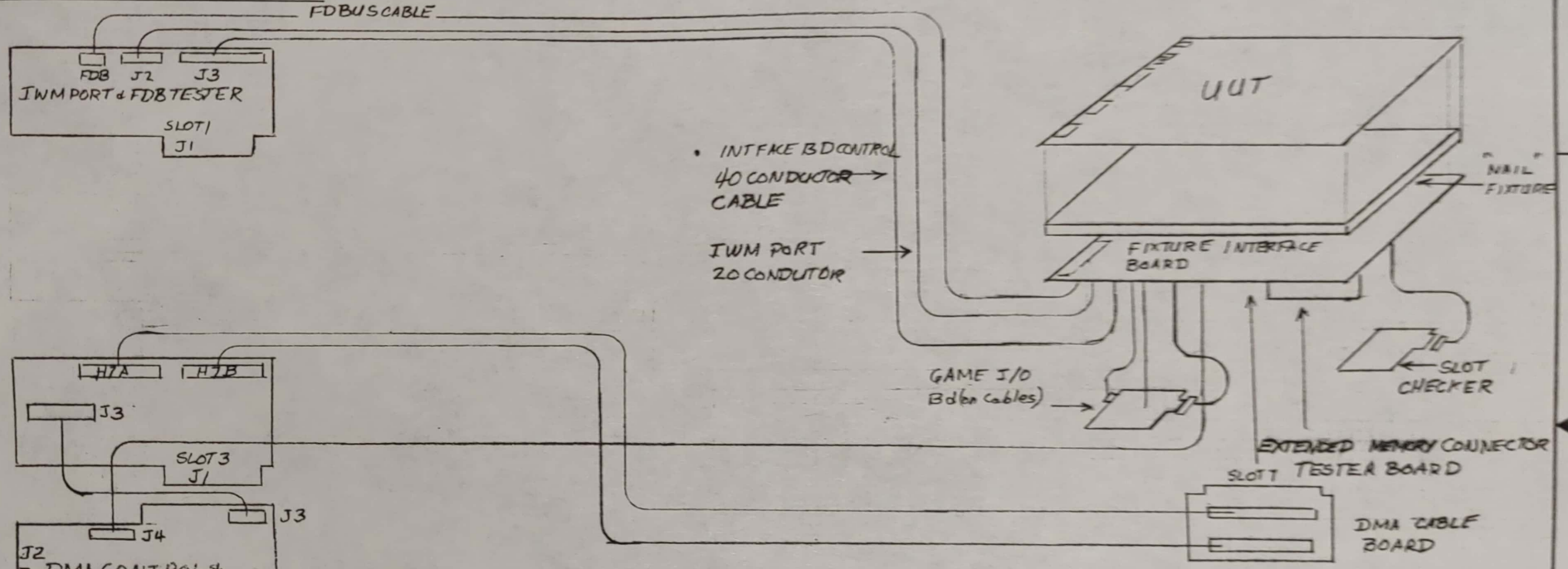
Karl Grabe
Apple Computer Inc..
Mail Stop: 22L, 20525 MARIANI AVE
CUPERTINO, CALIFORNIA 95014
USA


SYSTEST

replace

NOTE: UNLESS OTHERWISE SPECIFIED

REV.	ZONE	ECO #	REVISION	APPD



THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.
DECIMALS .X ± ____ .XX ± ____ .XXX ± ____
ANGLES XX.X ± ____
FRACTIONS ± ____
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.

DRAWN BY Mike Collins DATE 12/17/85
CHECKED BY DATE
APPROVED BY DATE
RELEASED BY DATE

apple computer inc.

TITLE BOARD TEST CABLE CONFIGURATION

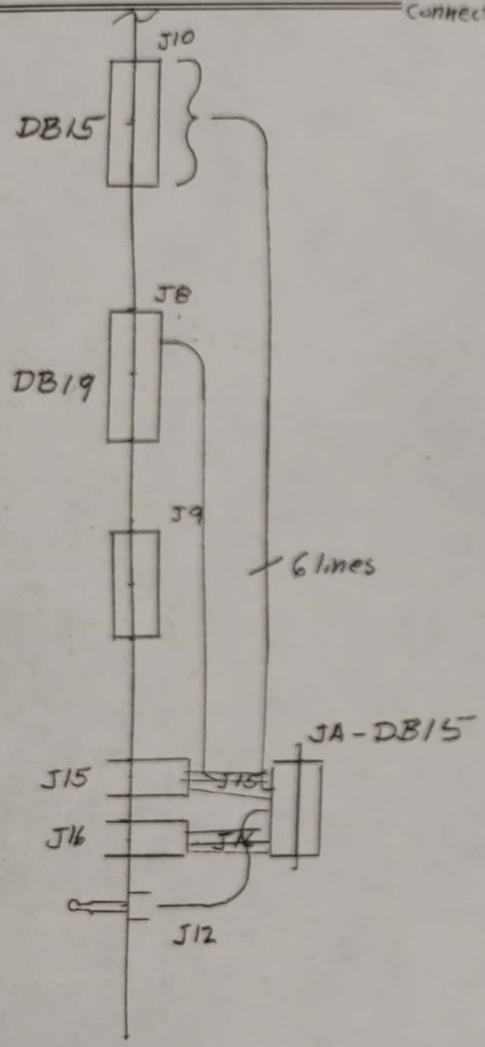
SIZE B
DRAWING NUMBER TSKA 002Z

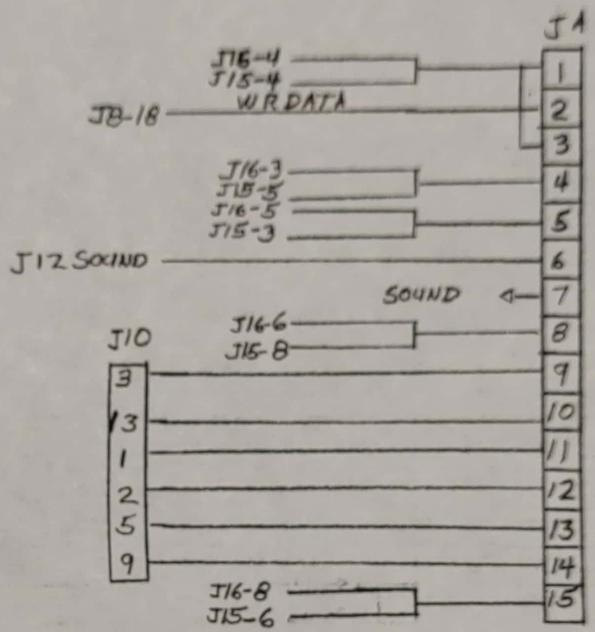
MATERIAL:
NEXT ASSY.
FINISH:
SCALE: 1/2 approx
SHEET OF

DRAWING NUMBER
SH OF

REV.	ZONE	ECO #	REVISION	APPD

NOTE: UNLESS OTHERWISE SPECIFIED Front Desk Bus and Video connector Not shown.





ITEM	QTY	PART NUMBER	DESCRIPTION

THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

TOLERANCES
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
DECIMALS .X ± ___ .XX ± ___ .XXX ± ___
ANGLES XX.X ± ___
FRACTIONS ± ___
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.

DRAWN BY Mike Collins DATE 12/18/85
CHECKED BY DATE
APPROVED BY DATE
RELEASED BY DATE

apple computer inc.

TITLE
WIRING DIAGRAM SYSTEM TEST CONNECTOR ASSEMBLY

SIZE B
DRAWING NUMBER TSKA0024

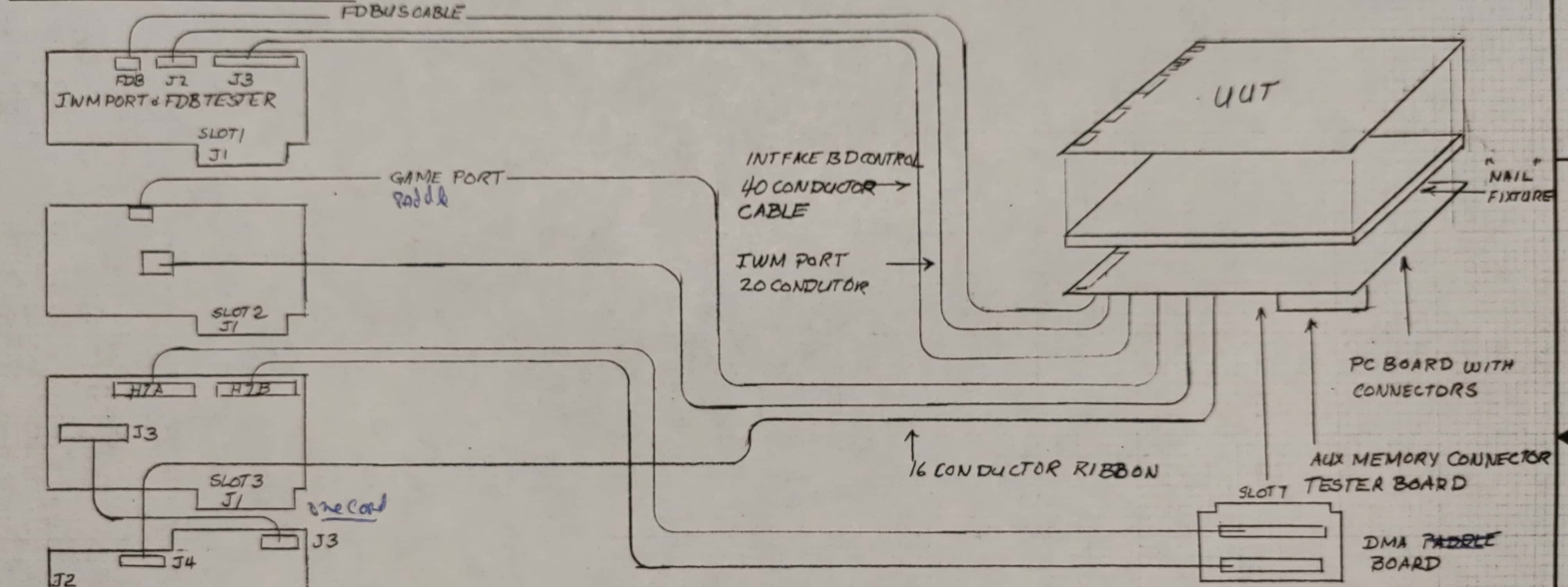
MATERIAL:
NEXT ASSY.
FINISH:
SCALE:
SHEET / OF /

DRAWING NUMBER
SH
OF


BDTEST

REV.	ZONE	ECO #	REVISION	APPD

NOTE: UNLESS OTHERWISE SPECIFIED



ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
DECIMALS .X ± ____ .XX ± ____ .XXX ± ____
ANGLES XX.X ± ____
FRACTIONS ± ____
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.

THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

DRAWN BY Mike Collins DATE 12/17/85
CHECKED BY DATE
APPROVED BY DATE
RELEASED BY DATE

MATERIAL:
NEXT ASSY. FINISH:

apple computer inc.

TITLE BOARD TEST CABLE CONFIGURATION

SIZE B | DRAWING NUMBER TSKA 0022

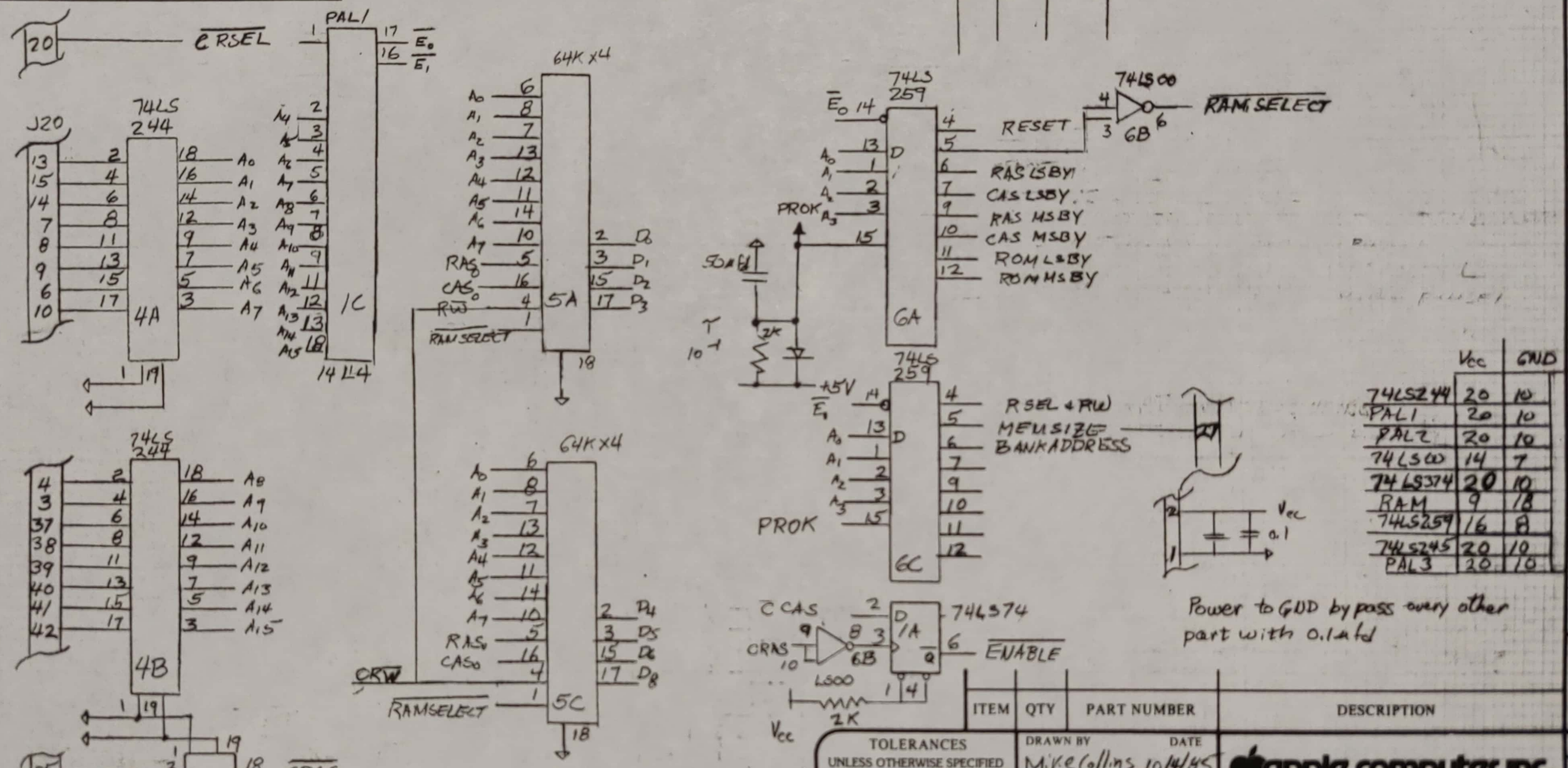
SCALE: 1/2 approx | SHEET OF

DRAWING NUMBER SH OF

AUX RMT ST

NOTE: UNLESS OTHERWISE SPECIFIED

REV.	ZONE	ECO #	REVISION	APPD
11/6/85			Ref Designators + ROM Bank logic 7A 7B	



	Vcc	GND
74LS244	20	10
PAL1	20	10
PAL2	20	10
74LS00	14	7
74LS374	20	10
RAM	9	18
74LS259	16	8
74LS245	20	10
PAL3	20	10

ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES
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DECIMALS .X ± ____ .XX ± ____ .XXX ± ____
ANGLES XX.X ± ____
FRACTIONS ± ____
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.

THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

DRAWN BY Mike Collins DATE 10/14/85
CHECKED BY DATE
APPROVED BY DATE
RELEASED BY DATE

MATERIAL:
FINISH:
NEXT ASSY.

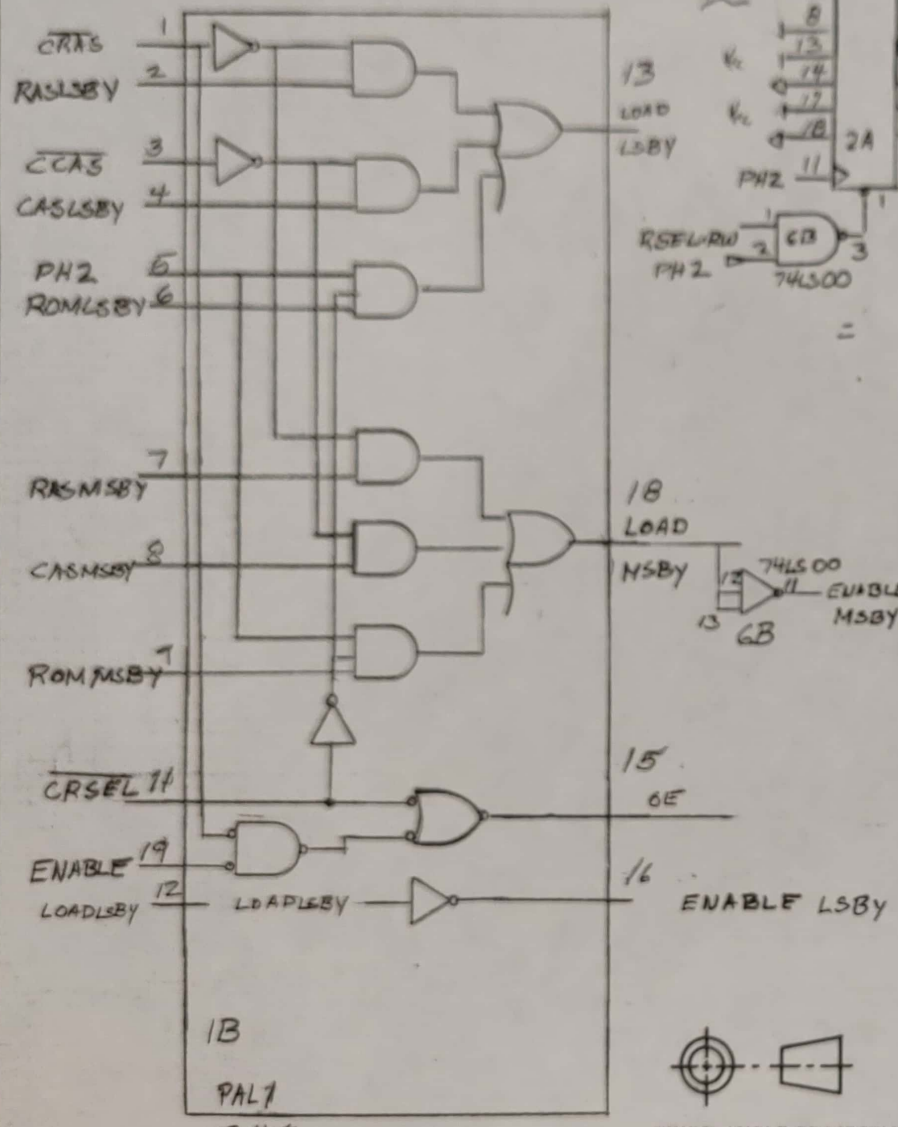
apple computer inc.

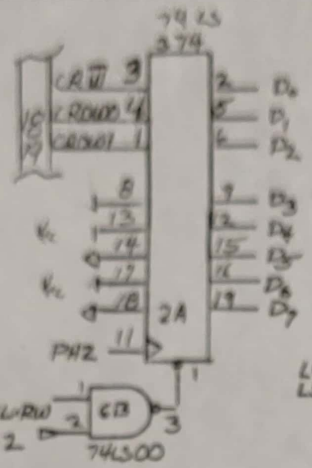
TITLE Aux Memory Tester Card

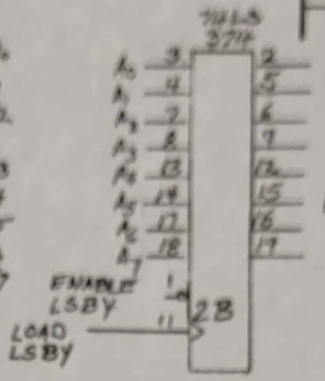
SIZE B
DRAWING NUMBER 73KA 0001
SCALE:
SHEET 1 OF 2

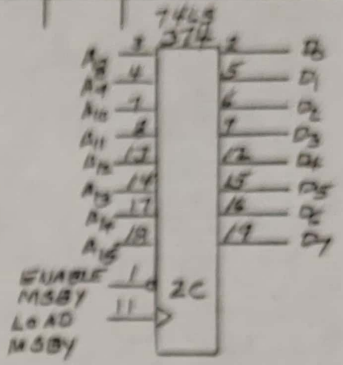
DRAWING NUMBER
SH OF

NOTE: UNLESS OTHERWISE SPECIFIED









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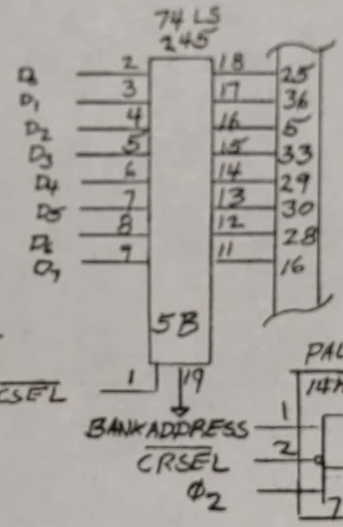

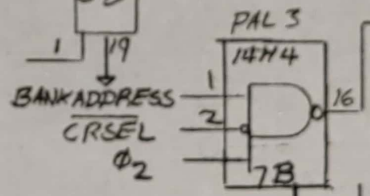

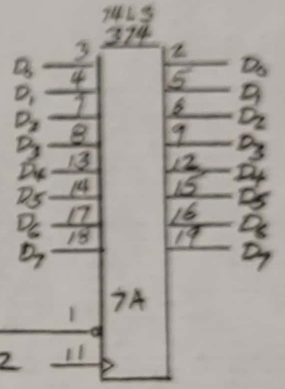

THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

REV	ZONE	ECO #	REVISION	APPD

ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.
DECIMALS .X ± ___
.XX ± ___
.XXX ± ___
ANGLES XX.X ± ___
FRACTIONS ± ___
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.

DRAWN BY Mike Collins DATE 10/4/85
CHECKED BY DATE
APPROVED BY DATE
RELEASED BY DATE

apple computer inc.

TITLE Aux Memory Test Card

SIZE B
DRAWING NUMBER 7SKA 0001.

MATERIAL:
FINISH:
NEXT ASSY.
SCALE:
SHEET 2 OF 2

TO: Randy Carr

FROM: Mike Collins 12/17/85

SUBJECT: Aux Ram Slot Test guidlines.

TSKA 0023

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OVERVIEW:

The card contains ram and a bank of softswitches for testing the auxillary memory slot functionally. There is a 64K by 8 bit memory on the board mapped into the memory space as documented below. To control the mode of the card there is a bank of 32 soft switches that allow the test to be switched into varous modes. The philosophy is to test the slot by feeding addresses back into the data bus from the address bus. The softswitches control which byte of the address field is read onto the data bus and there is a mode where the card will act like a ram such that a memory diagnostic can be done.

SOFTSWITHES:

The softswithes can be accessed in any bank of ROM that decodes to the auxilary memory space. I used F0 to check out the card. The first 32 (1F in hex) addresses in the ROM bank, address the soft swithes. All even addresses clear the swithes. After power up it is a good idea to address each of the even addresses in the first 32 to clear the switches. After this the switches can be set as needed. The function of each odd switch is documented below. The even address below these odd addresses will clear the switch:

ADDRESS	FUNCTION
01	NU
03	Select RAM mode of operation. Must be turned on for card to act like a RAM.
05	RAS LSBY. Card reads back RAS address when a read is done from a RAM bank in AUX space.
07	CAS LSBY. Reads back CAS address. This includes some bank address information. See below.

09	RAS MSBY. Reads back Upper RAS address. This has the upper 2 bits of the RAS address.
0B	CAS MSBY. Reads back upper 2 bits of CAS.
0D	ROM LSBY. Reads back first 8 bits
0F	ROM MSBY. Reads back 2nd 8 bits.
11	RSEL AND RW. Reads back bank select Returns RAM bank address. RW will always be in read postion.
13	MEMSIZE Forces memsize [illegible] changes the bank map.
15	BANK ADDRESS. Reads back the bank address that comes down the data bus during the access cycle when PH2 is high. Used for reading ROM bank select.

All of the above modes must be cleared before another one can be selected. The only exception is the MEMSIZE bit which can be in either position.

BANK ADDRESS:

Bank address for ram varies depenting on MEM SIZE bit. The least signifigant 8 bits of address are presented to the card using the RAS falling edge. The other addresses are not so straight forward. The use of diagrams is the only way to explain the address mapping situation.

9 Bit address field or 256K ram mode. Set MEMSIZE = 1. The address field looks like:

RAS 2^8 2^7 2^6 2^5 2^4 2^3 2^2 2^1 2^0

CAS B1 2^{15} 2^{14} 2^{13} 2^{12} 2^{11} 2^{10} 2^9 B0

The right most 8 bits are presented to the data bus by RAS LSBY and CAS LSBY softswitches (05 or 07 swithes).
B2 is ignored in this mode but the card presents B2 to the bus in the D1 data position when the CAS MSBY (soft switch 0B) is read. This signal is simply not wired in the current version of the 256 memory card. B4 and B3 are in the Row select word. That is the word that is read back after soft switch 11 is set. The format of the CAS MSBY word is:

X X X X X X B2 B1

And the format of the Row select word is:

0 1 0 1 0 B4 B3 1

The least significant bit is actually the position of the RW line; since it is impossible to read from the card when the RW line is in a state other than the read state we always sense a 1.

10 bit address field or 1 meg ram mode. MEM SIZE = 0.
The address field is:

RAS	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
CAS	B2	B1	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	B3	B0

As before the RAS LSBY and CAS LSBY words will feed back the right most 8 bits. The 2 bits on the left are available from RAS and CAS MSBY. The format of the Row select word is the same as before except B4 and B5 appear in the bit positions D1 and D2.

0 1 0 1 0 B5 B4 1

ROM SPACE:

Rom addresses can be read back by setting the appropriate switches and getting the address on the bus. The only complication is that one should avoid using the first addresses because it could possibly affect the position of the soft swithes.

EXAMPLES:

With MEM SIZE = 1 (9 bit address field)

CAS LSBY is even for even banks and odd for odd banks. That is B0 is lsbit.

B1 comes out as Msbit.

The Row select word works as follows:

```
read from bank 02 read 51
read from bank 03 read 51
read from bank 04 read 53
read from bank 05 read 53 ?
read from bank 06 read 53
read from bank 07 read 53
read from bank 08 read 55
               09      55
               0A      55
               0B      55
               0C      57
```

0D	57
0E	57
0F	57
10	51
20	51
30	51
3F	57

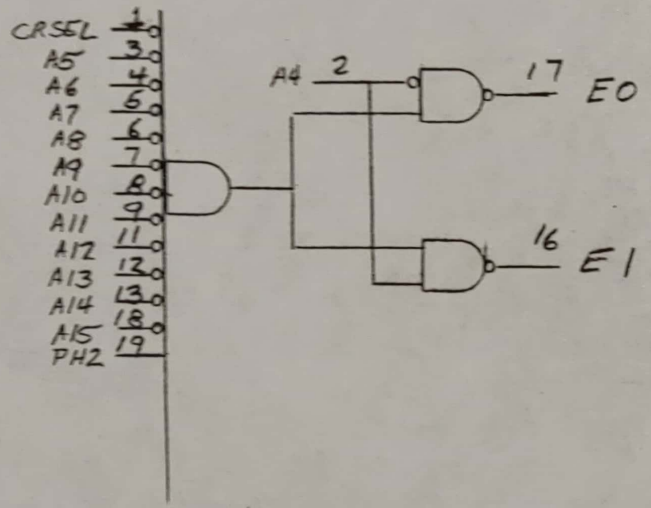
Because B1 is ignored by the test card, the ram card does not distingish between adjacent 256 word blocks. Therefore the second 256 word block is a copy of the first. The memory map continues up to 128k above 020000 (in Hex). Bank 03 will be unique from bank 02 because the 64K of ram will be spread over 128K. Since the ram has no bank address decoded to chip select it all banks above in the RAM memory map will be copies of banks 02 and 03. There doesn't have to be a detailed diagnostic of all this space but a reasonably complex combination of addresses and bank addresses should be tried such that the hardware is proven to be free of shorts, opens and pattern sensitivities.

MEM SIZE = 0 EXAMPLES:

Since B3 is brought into the second position of CAS we change the way that the on board memory maps. In this case we keep 256 word unique blocks. This time there will be four blocks of 256 words that are tied together. We will observe unique ram locations in 256 words out of each 1024. The bank address lines B1 and B2 are ignored. Therefore there will be 4 64K word copies between unique ram blocks. That is banks 02 03 04 and 05 will be mirrored by 06 07 08 and 09.

NOTE: UNLESS OTHERWISE SPECIFIED

PAL1 & PAL3 ARE DRAWN ON SCHEMATIC



REV.	ZONE	ECO #	REVISION	APPD

ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
DECIMALS .X ± ____ .XX ± ____ .XXX ± ____
ANGLES XX.X ± ____
FRACTIONS ± ____
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.

DRAWN BY DATE
CHECKED BY DATE
APPROVED BY DATE
RELEASED BY DATE

apple computer inc.

TITLE PAL EQUATIONS AND LOGICAL EQUIVALENTS AUX MEM TESTER

SIZE B | DRAWING NUMBER TSKA 0026

MATERIAL:

NEXT ASSY. | FINISH:

SCALE: | SHEET 2 OF 2

THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

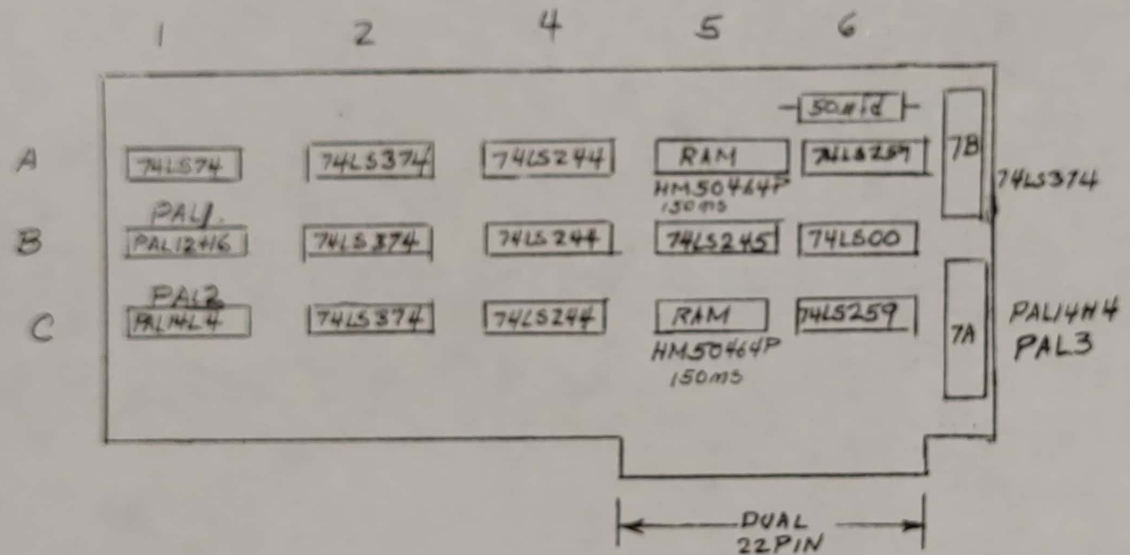
DRAWING NUMBER | SH | OF

D C A

4 3 2 1

REV	ZONE	ECO #	REVISION	APPD

NOTE: UNLESS OTHERWISE SPECIFIED



ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.
DECIMALS .X ± ____
.XX ± ____
.XXX ± ____
ANGLES XX.X ± ____
FRACTIONS ± ____
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.

DRAWN BY Mike Collins DATE 1/6/86
CHECKED BY DATE
APPROVED BY DATE
RELEASED BY DATE

apple computer inc.

TITLE LAYOUT: EXTENDED MEMORY BD

SIZE B
DRAWING NUMBER TSKA 0031

MATERIAL:
FINISH:
NEXT ASSY.
SCALE:
SHEET 1 OF 1

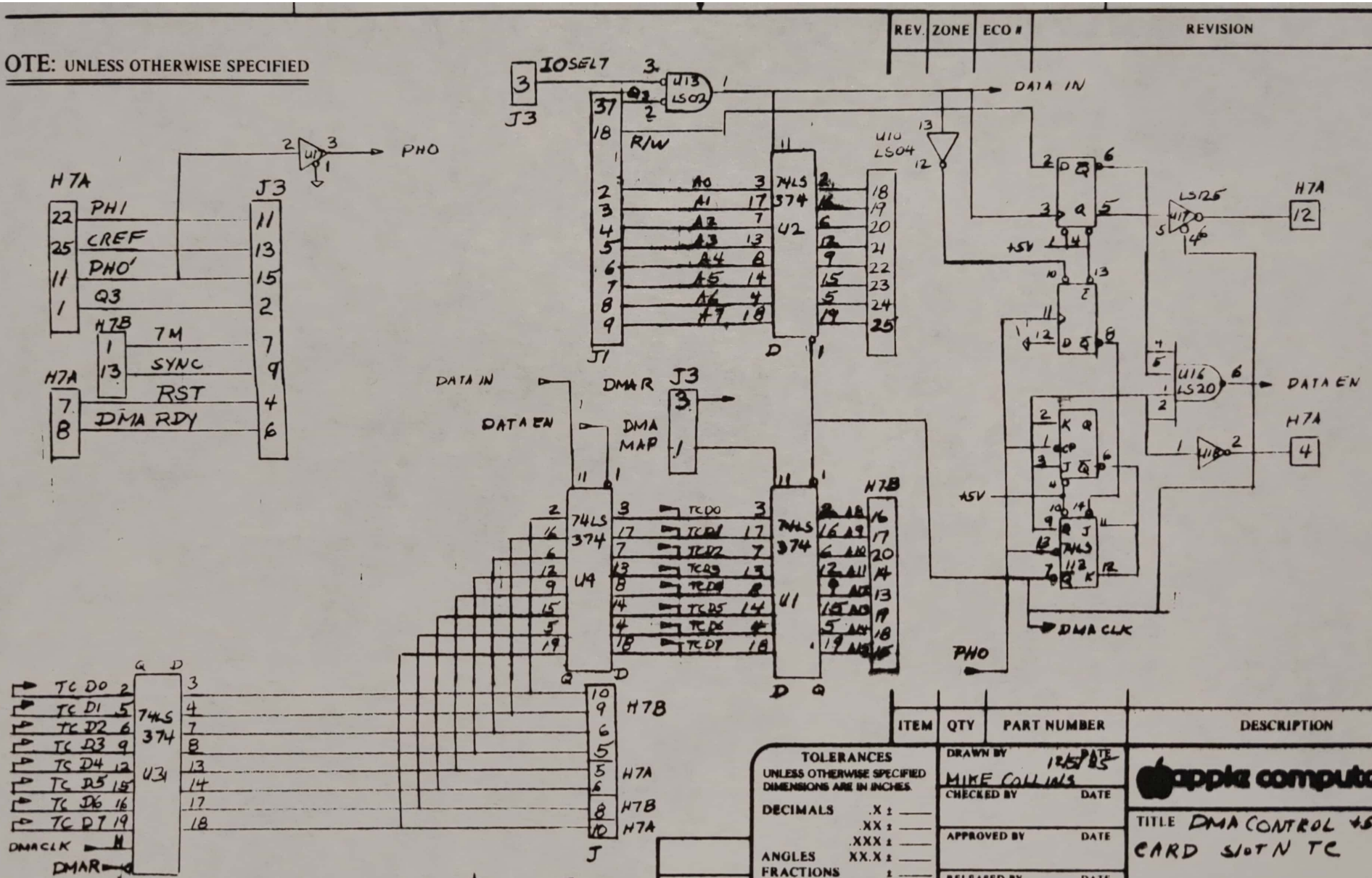
THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

DRAWING NUMBER
SH OF


DMA BD

OTE: UNLESS OTHERWISE SPECIFIED

REV.	ZONE	ECO #	REVISION	APPD



THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
DECIMALS .X ± .1 .XX ± .01 .XXX ± .005
ANGLES XX.X ± 1°
FRACTIONS ± 1/64
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.

DRAWN BY MIKE COLLINS DATE 12/5/85
CHECKED BY DATE
APPROVED BY DATE
RELEASED BY DATE

apple computer inc.

TITLE DMA CONTROL SIGNATURE CARD SLOT N TC

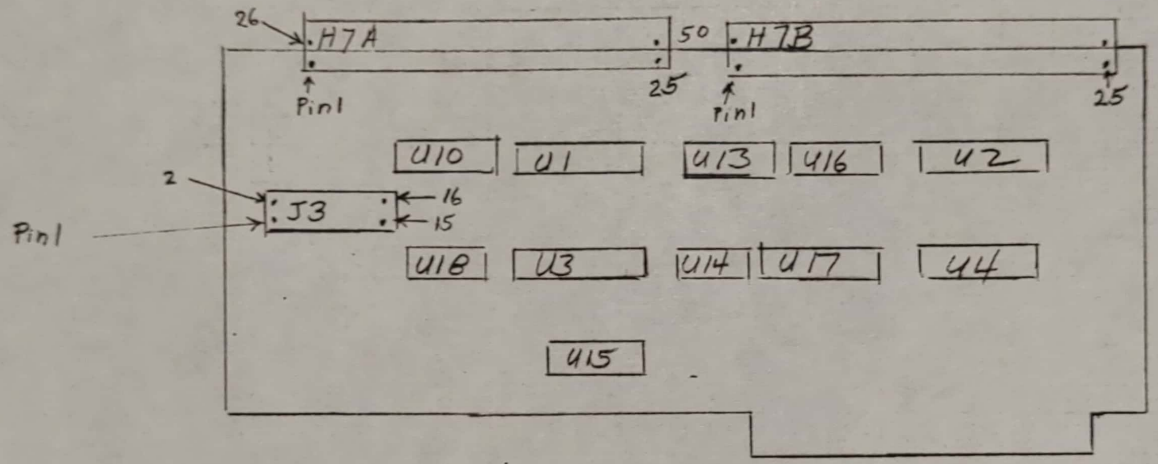
SIZE B
DRAWING NUMBER TSKA 0017

MATERIAL:
FINISH:
NEXT ASSY.
SCALE:
SHEET 1 OF 1

4 3 2 1

NOTE: UNLESS OTHERWISE SPECIFIED

REV.	ZONE	ECO #	REVISION	APPD



ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.
DECIMALS .X ± ____
.XX ± ____
.XXX ± ____
ANGLES XX.X ± ____
FRACTIONS ± ____
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.

DRAWN BY MIKE COLLINS DATE 12/6/85
CHECKED BY DATE
APPROVED BY DATE
RELEASED BY DATE

apple computer inc.

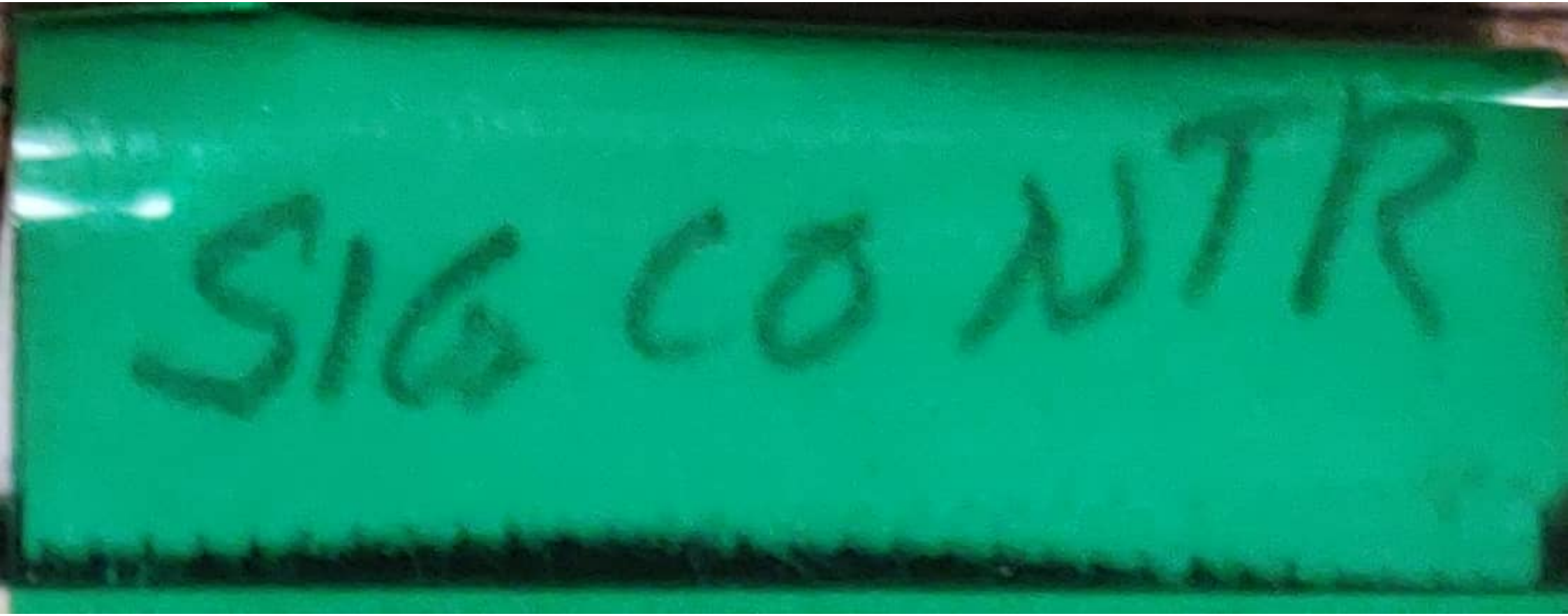
TITLE PARTS PLACEMENT FOR DMA CARD

SIZE B
DRAWING NUMBER TSKA 0019

MATERIAL:
FINISH:
NEXT ASSY.
SCALE:
SHEET / OF /

THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

DRAWING NUMBER
SH OF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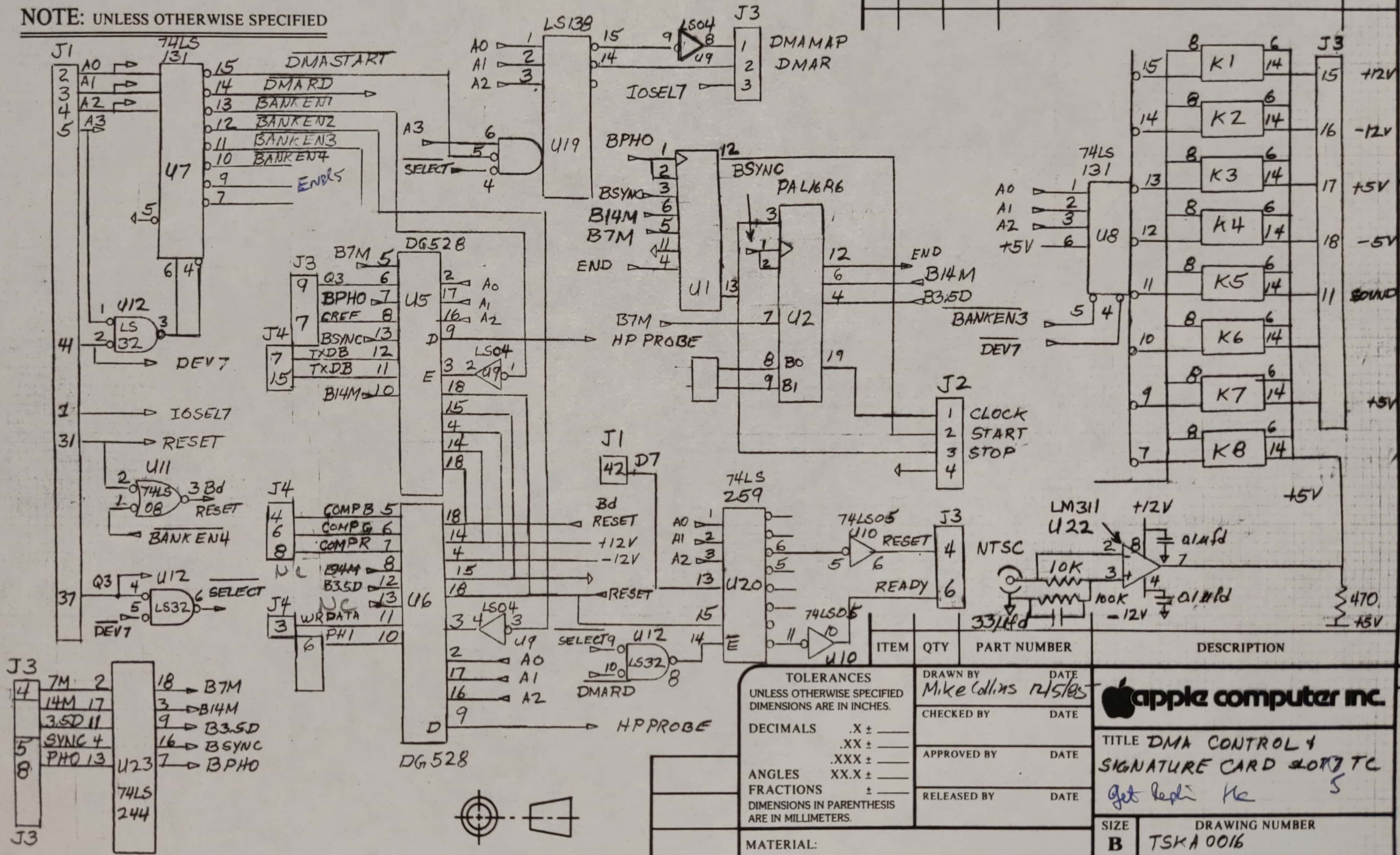
NOTE: UNLESS OTHERWISE SPECIFIED

REV.	ZONE	ECO #	REVISION	APPD



THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
DECIMALS .X ± .XX ± .XXX ±
ANGLES XX.X ±
FRACTIONS ±
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.

MATERIAL:

NEXT ASSY. FINISH:

DRAWN BY Mike Collins DATE 12/5/85
CHECKED BY DATE
APPROVED BY DATE
RELEASED BY DATE

apple computer inc.

TITLE DMA CONTROL & SIGNATURE CARD SLOT 7 TC 5
Get Repli Kc

SIZE B DRAWING NUMBER TSKA 0016

SCALE: SHEET 1 OF 2

```
 1 PAL16R4
 2 4 BIT COUNTER WITH RS LATCH TO CREATE STRART AND STOP FOR SIGNATURE
 3 ANALYSIS.  COUNTER DECODES THE EVENT THAT SYNC IS LOW FOR MORE THAN
 4 4 PH0 PERIODS.
 5 BPH0 PH0 SYNC END M7 M14 NU7 NU8 NU9 GND EN /START /STOP /C0 /C1 /C2 /C3
   NU18 NU19 VCC
 6 C0  := /C0*/SYNC
 7 C1  := /C0*C1*/SYNC+C0*/C1*/SYNC
 8 C2  := C0*C1*/C2*/SYNC+/C0*C2*/SYNC+/C1*C2*/SYNC
 9 C3  := C0*C1*C2*/C3*/SYNC+/C0*C3*/SYNC+/C1*C3*/SYNC+/C2*C3*/SYNC
10 STOP = C0*/C1*/C2*C3*/PH0+START
11 START =/END+STOP
12 DESCRIPTION
```

```
 1 PAL16R6
 2 6 BIT COUNTR
 3
 4
 5 A BS S B3.5D NU5 BM14 BM7 B0 B1 GND EN END /C0 /C1 /C2 /C3 /C4 /C5 SIGC V
   CC
 6
 7 C0  := /C0*S
 8 C1  := /C0*C1*S+C0*/C1*S
 9 C2  := C0*C1*/C2*S+/C0*C2*S+/C1*C2*S
10 C3  := C0*C1*C2*/C3*S+/C0*C3*S+/C1*C3*S+/C2*C3*S
11 C4  := C0*C1*C2*C3*/C4*S+/C0*C4*S+/C1*C4*S+/C2*C4*S+/C3*C4*S
12 SIGC = /B1*/B0*/BM7+/B1*B0*/BM14+B1*/B0*/BS+B1*B0*/B3.5D
13 C5:=C0*C1*C2*C3*C4*/C5*S+/C0*C5*S+/C1*C5*S+/C2*C5*S+/C3*C5*S+/C4*C5*S
14 END = C0*C1*C2*C3*C4*C5*/BS
15 DESCRIPTION
```

Mike Collins
1/3/86

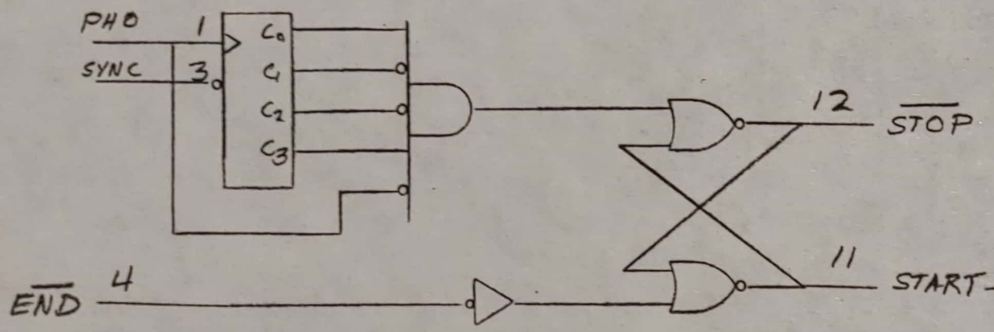
PAL EQUATIONS AND
LOGICAL EQUIVALENTS
DMA CONTROL BOARD

TSKA 0027

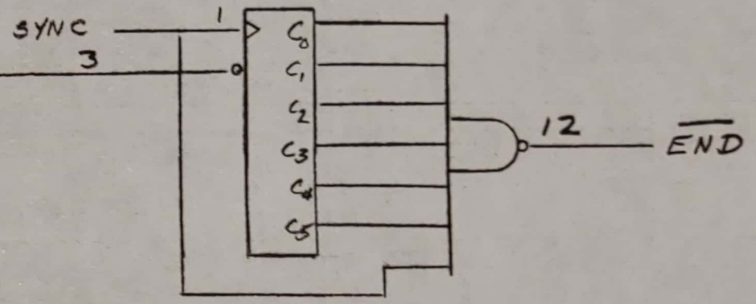
REV.	ZONE	ECO #	REVISION	APPD

NOTE: UNLESS OTHERWISE SPECIFIED

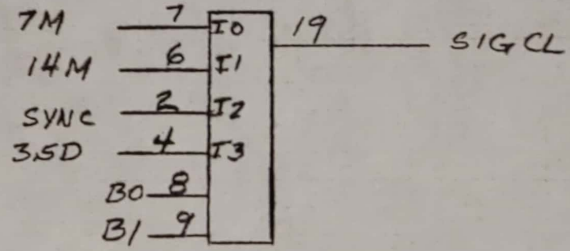
4 BIT COUNTER PAL



6 BIT COUNTER PAL



ADDITIONAL FUNCTION
OF 6 BIT CNTR
SELECTS 1 of 4 clocks



ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.
DECIMALS .X ± ___ .XX ± ___ .XXX ± ___
ANGLES XX.X ± ___
FRACTIONS ± ___
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.

DRAWN BY Mike Collins DATE 11/3/86
CHECKED BY DATE
APPROVED BY DATE
RELEASED BY DATE

MATERIAL:
FINISH:
NEXT ASSY.

apple computer inc.

TITLE PAL EQUATIONS AND LOGICAL EQUIVALENTS DMA CONTROL BD

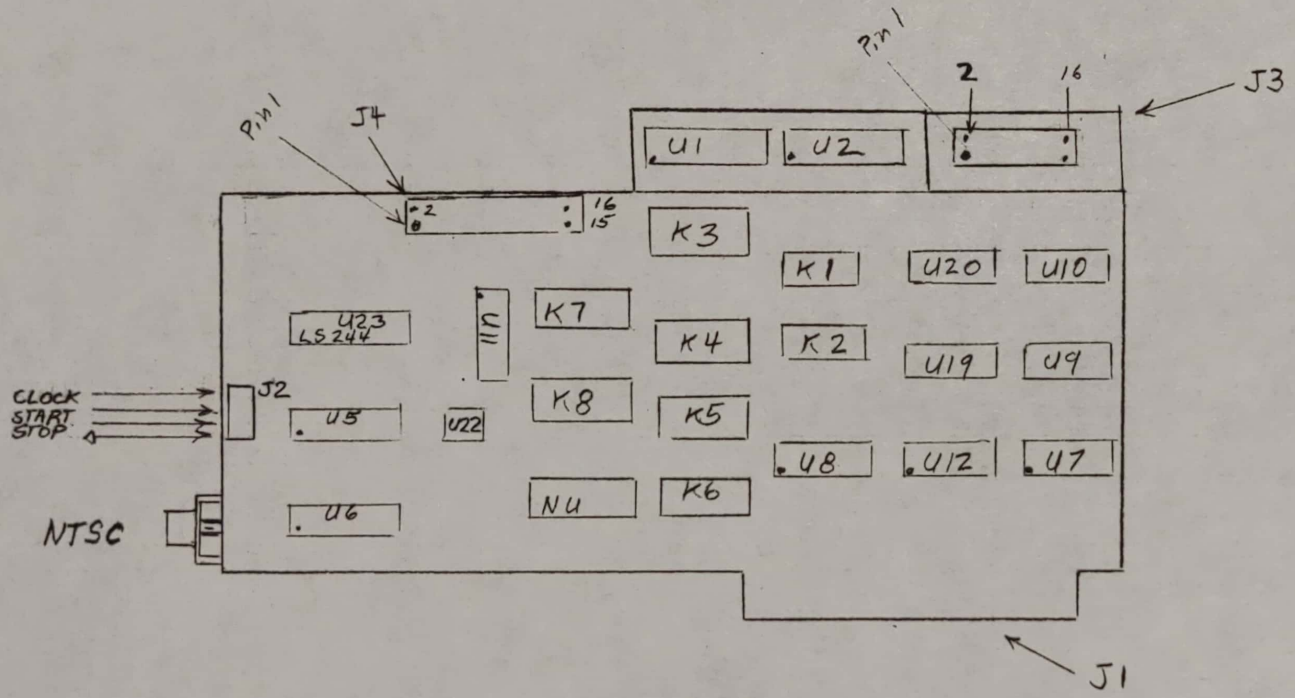
SIZE B
DRAWING NUMBER TSKA 0027
SCALE:
SHEET 2 OF 2

THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

DRAWING NUMBER
SH OF

NOTE: UNLESS OTHERWISE SPECIFIED

REV.	ZONE	ECO #	REVISION	APPD



ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.
DECIMALS .X ± ____
.XX ± ____
.XXX ± ____
ANGLES XX.X ± ____
FRACTIONS ± ____
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.

DRAWN BY Mike Collins DATE 12/10/85
CHECKED BY DATE
APPROVED BY DATE
RELEASED BY DATE

apple computer inc.

TITLE DMA CONTROL & SIGNATURE CARD LAYOUT DRAWING

SIZE B
DRAWING NUMBER TSKA 0018

MATERIAL:
NEXT ASSY.
FINISH:
SCALE:
SHEET 1 OF 1

THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

DRAWING NUMBER SH OF

To: KC Tan

From: Mike Collins 1/5/86

Subject: Changes in softswitches in signature tree.

==========

Because of the differences in the new product from the Apple IIE, several changes have been made from the previous assignments in the signature relay tree. As before the banks are selected by doing a memory access, usually a LDA, to $C0F2, $C0F3, $C0F4 to get Bank1, Bank2, and Bank3 respectively. The new assignments follow the old as much as possible.

Bank 1

$C0F8	7M (FREQ)
$C0F9	Q3 (FREQ)
$C0FA	PH0 (FREQ)
$C0FB	CREF (FREQ)
$C0FC	SYNC (?)
$C0FD	TXDA (SIGNATURE)
$C0FE	TXDB (SIGNATURE)

TXDA and TXDB are the serial outputs of the ports J15 and J16. The signature capability is there to use if a diagnostic mode is necessary.

$C0FF	UNASSIGNED

Bank 2:

$C0F8	COMP RED (SIGNATURE)
$C0F9	COMP GREEN (SIGNATURE)
$C0FA	COMP BLUE (SIGNATURE)
$C0FB	UNASSIGNED
$C0FC	3.5D

This signal is here to be used for board test. The VGC can be forced into test mode where 3.5D becomes a clock for composite video.

$C0FD	14M (FREQUENCY)
$C0FE	WRDA (SIGNATURE)

WRDA is the data from the IWM port.

$C0FF	PH1 (FREQUENCY)

Bank 3.

$C0F8	UUT 12V
$C0F9	UUT -12V
$C0FA	UUT 5V
$C0FB	UUT -5V
$C0FC	SOUND

Sound can be checked by doing a frequency measurement and a peak to peak

voltage measurement.

$COFD & $COFE	UNASSIGNED
$COFF	NTSC without sync

NTSC without sync will give a signature in the old video modes using 14M as the clock. To get a signature from new video modes the VGC will have to be placed in test mode. 3.5D will give a clock that can be used to take signatures on video. This is true for both composite video and RGB video. (Note that the test point to force VGC test mode is not available at the system level.) I propose that we do new video modes at board test and take signatures on old video modes during system test.

A feature that I added that you may choose to use is a 4 to 1 selector for the clock for signature. The choices are 14M, 7M, Composite SYNC, and 3.5D. The 3.5D I am sure you will use for board test. The slower clocks will allow us to get stable signatures on signals that come through all the cables.

The other features of the board remain the same except for the cable configuration and the way that the start-stop signal is made for signatures.

The PALs I added in place of the 74LS161 will create a start stop window. These are documented elsewhere.

```
1 PAL12H6
2 PAL1
3 M. COLLINS
4
5 CRAS RASLSBY CCAS CASLSBY PH2 ROMLSBY RASMSBY CASMSBY ROMMSBY GND CRSEL I
  LDLSBY LDLSBY NU14 OE ENLSBY NU1 LOADMSBY ENABLE VCC
6
7 LDLSBY = /CRAS*RASLSBY+/CCAS*CASLSBY+PH2*ROMLSBY*/CRSEL
8 LOADMSBY = /CRAS*RASMSBY+/CCAS*CASMSBY+PH2*ROMMSBY*/CRSEL
9 OE = CRAS*CRSEL+ENABLE*CRSEL
10 ENLSBY  = /ILDLSBY
11 DESCRIPTION
12
13
14
```

```
1 PAL14L4
2 DECODER
3 M.COLLINS
4
5 CRSEL A4 A5 A6 A7 A8 A9 A10 A11 GND A12 A13 A14 NU1 NU2 E1 E0 A15 PH2 VCC

6 E0=/CRSEL*/A4*/A5*/A6*/A7*/A8*/A9*/A10*/A11*/A12*/A13*/A14*/A15*PH2
7 E1=/CRSEL*A4*/A5*/A6*/A7*/A8*/A9*/A10*/A11*/A12*/A13*/A14*/A15*PH2
8 DESCRIPTION
9
```

```
1 PAL14H4
2 MIKE COLLINS 11/3/85
3 ADDITIONAL PAL TO CONTROLL BANK ADDRESS
4 NU
5 BNKADDR CRSEL PH2 RW E0 E1 NU7 NU8 NU9 GND NU11 NU12 NU13 EN0 EN1 BNKEN N
  U17 NU18 NU19 VCC
6 BNKEN =  /BNKADDR+CRSEL+/PH2
7 EN0 = E0+RW
8 EN1 = E1+RW
9 DESCRIPTION
```

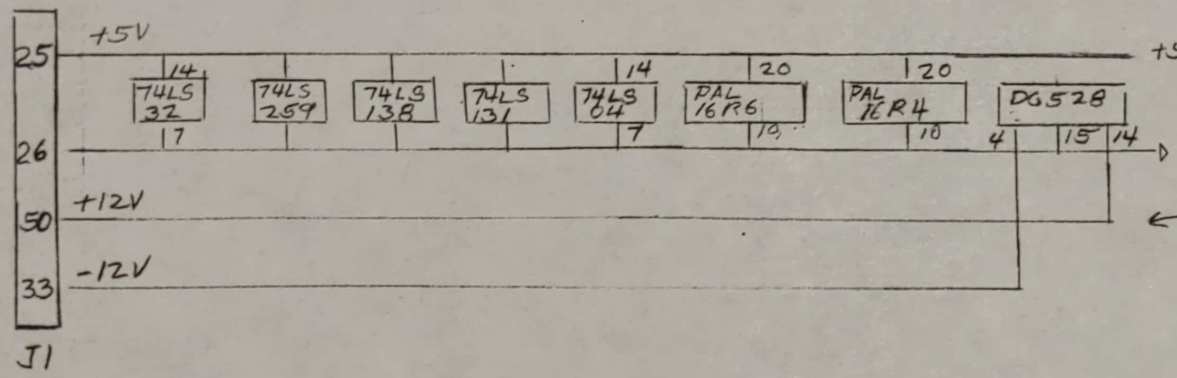
Mik Collins
1/3/86

PAL EQUATIONS
AND LOGICAL
EQUIVALENTS
AUX MEM TESTER

TSKA 0026

NOTE: UNLESS OTHERWISE SPECIFIED

REV.	ZONE	ECO #	REVISION	APPD



ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.
DECIMALS .X ± ____
.XX ± ____
.XXX ± ____
ANGLES XX.X ± ____
FRACTIONS ± ____
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.

DRAWN BY DATE
CHECKED BY DATE
APPROVED BY DATE
RELEASED BY DATE

apple computer inc.

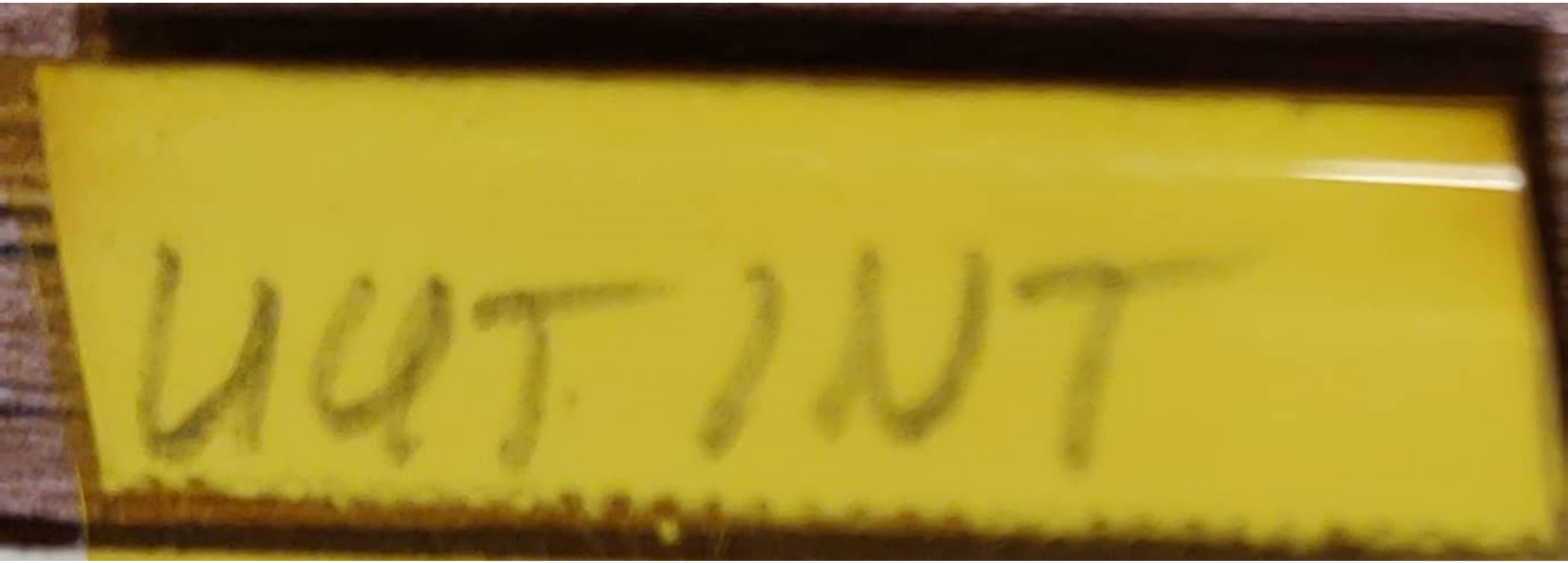
TITLE DMA CONTROL & SIGNATURE CARD SLOT 7 TC

SIZE B
DRAWING NUMBER TSKA 0016

MATERIAL:
FINISH:
NEXT ASSY.
SCALE:
SHEET 2 OF 2

THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

DRAWING NUMBER
SH OF

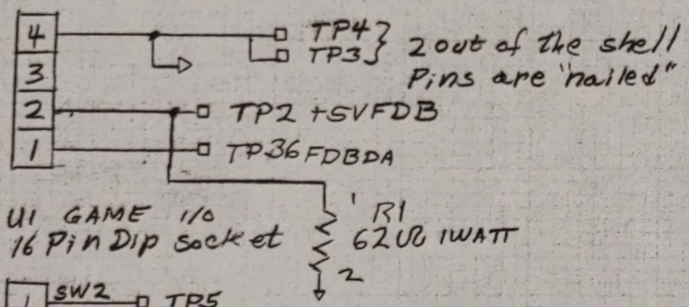

UNIT

NOTE: UNLESS OTHERWISE SPECIFIED

KEYBOARD CONNECTOR J13 26 Pin

REV.	ZONE	ECO #	REVISION	APPD
			REVISION HISTORY ON PG 6	

J18 Mini Din 4Pin
Front Dask Bus



1	SW2	TP5
2	SW1	TP6
3	SW0	TP7
4	+5V	TP8
5	STBL	TP9
6	PDL0	TP10
7	PDL2	TP11
8		TP12
9	PDL1	TP32
10	PD4	TP14
11	PD3	TP15
12	AN3	TP16
13	AN2	TP17
14	AN1	TP18
15	AN0	TP19
16		TP20

1	Y0	TP319
2	Y1	TP320
3	+5V	TP321
4	Y2	TP322
5	KSW1	TP323
6	Y3	TP324
7	KSW0	TP325
8	Y4	TP326
9	CAPLOCK	TP327
10	Y5	TP328
11	CNTRL	TP329
12	Y8	TP330
13	GND	TP331

14	X0	TP332
15		TP333
16	X2	TP334
17	X7	TP335
18	X1	TP336
19	X5	TP337
20	X3	TP338
21	X4	TP339
22	Y9	TP340
23	Y6	TP341
24	SHIFT	TP342
25	Y7	TP343
26	X6	TP344

NO ORIENTATION MARK!

ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
DECIMALS .X ± ____ .XX ± ____ .XXX ± ____
ANGLES XX.X ± ____
FRACTIONS ± ____
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.

DRAWN BY Mike Collins DATE 11/4/85
CHECKED BY DATE
APPROVED BY DATE
RELEASED BY DATE

apple computer inc.

TITLE
UUT INTERFACE BOARD

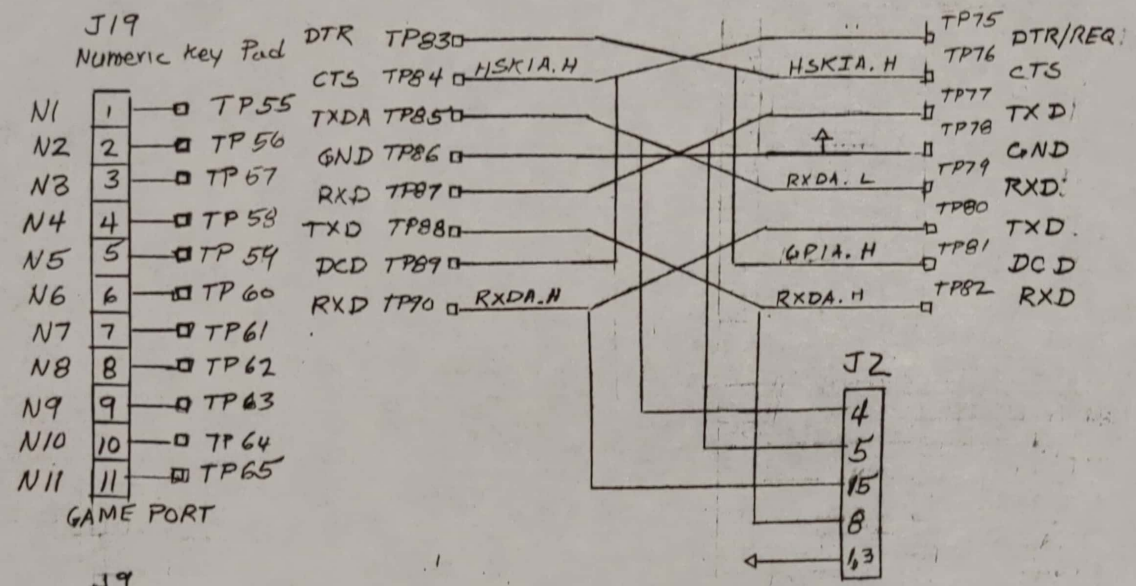
SIZE B
DRAWING NUMBER TSA0013

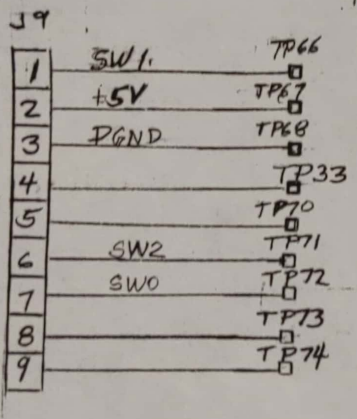
MATERIAL:
FINISH:
NEXT ASSY.
SCALE:
SHEET 1 OF 6

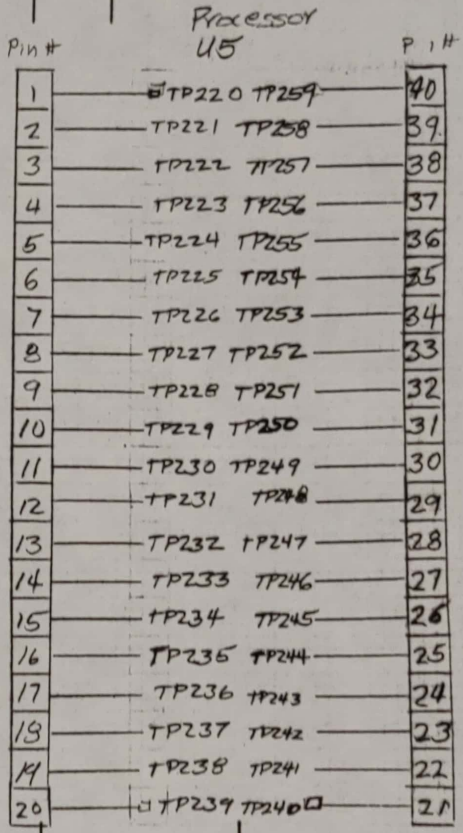
DRAWING NUMBER
SH 1 OF

THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

NOTE: UNLESS OTHERWISE SPECIFIED







REV.	ZONE	ECO #	REVISION	APPD

ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES
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.XX ± ____
.XXX ± ____
ANGLES XX.X ± ____
FRACTIONS ± ____
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DRAWN BY Mike Collins DATE 11/11/85
CHECKED BY DATE
APPROVED BY DATE
RELEASED BY DATE

apple computer inc.

TITLE
UUT INTERFACE BOARD

SIZE B
DRAWING NUMBER TSKA 0013

MATERIAL:
FINISH:
SCALE:
SHEET 2 OF 6
NEXT ASSY.

THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

NOTE: UNLESS OTHERWISE SPECIFIED

REV.	ZONE	ECO #	REVISION	APPD

J8 IWM PORT
DB19

3.5DIK3

1		TP181
2		TP182
3		TP183
4		TP184
5		TP185
6		TP186
7		TP187
8		TP188
9	DR2.L	TP189
10	WR PROTECT	TP190
11	PH0	TP191
12	PH1	TP192
13	PH2	TP193
14	PH3	TP194
15	WREQ	TP195
16	HDSEL.H	TP196
17	DR1.L	TP197
18	RD	TP198
19	WRDAT	TP199

J11 Monochrome Videout

1	VID	TP 300
2	VID GND	TP 301
3		TP 302

R3

RAS* — 2 — 220 — 1 — CLK

1		TP140
2		TP141
3	CASM*	TP142
4	Q	TP143
5	E	TP144
6	CSTRB	TP145
7	CA0	TP146
8	CA1	TP147
9	CA2	TP148
10	CA3	TP149
11	VREF	TP150
12	VLFDBK	TP151
13	VOL	TP152
14	WVREF	TP153
15	SIG+	TP154
16	SIG-	TP130
17		TP156
18	IRQ	TP157
19		TP158
20		TP159

+5V — 1K — 1% — R4 — 2 — 1K — 1 — 2 — R5 — 1K — 1% — 2 — TP37 J25-2

RES*

U4 ENSONICS

TP179	40	BS
TP178	39	C2 +5V 0.1
TP177	38	A_0
TP176	37	A_1
TP175	36	A_2
TP174	35	A_3
TP173	34	A_4
TP172	33	A_5
TP171	32	A_6
TP170	31	A_7
TP169	30	D0
TP168	29	D1
TP167	28	D2
TP166	27	D3
TP165	26	D4
TP164	25	D5
TP163	24	D6
TP162	23	D7
TP161	22	(WE*) R/W
TP160	21	CS*

DRAMS 64X4

U2 / U3

	U2	U3
A_0	6	6
A_1	8	8
A_2	7	7
A_3	13	13
A_4	12	12
A_5	11	11
A_6	14	14
A_7	10	10
RAS*	5	5
CAS	16	16
R/W	4	4
	1	1
	18	18
	9 C3 +5V	9 C1 +5V
D0	2	
D1	3	
D2	15	
D3	17	
D4		2
D5		3
D6		15
D7		17

TP180 — From UUT — CAS — R/W

ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES
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DECIMALS .X ± ____ .XX ± ____ .XXX ± ____
ANGLES XX.X ± ____
FRACTIONS ± ____
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.

DRAWN BY Mike Collins 11/11/85 DATE
CHECKED BY DATE
APPROVED BY DATE
RELEASED BY DATE

apple computer inc.

TITLE
UUT INTERFACE BOARD

SIZE B
DRAWING NUMBER TSKA 0013

MATERIAL:
NEXT ASSY.
FINISH:
SCALE:
SHEET 3 OF 6

THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

NOTE: UNLESS OTHERWISE SPECIFIED

J10 Video Connector
DB15

REV.	ZONE	ECO #	REVISION	APPD

1	GND	TP200
2	COMPRED	TP201
3	COMPSYNC	TP202
4		TP203
5	COMPGRN	TP204
6	GND	TP205
7		TP206
8	+12V	TP207
9	COMPBLUE	TP208
10		TP209
11	SOUND	TP210
12	COMPVID	TP211
13	GND	TP212
14		TP213
15		TP214

AUX MEMORY CONNECTOR
44 PIN J20

+5V	01	TP131	TP134	02	TP132	TP133	03	FABUS9	04	FABUS8	05	DBUS2	06	FABUS6	07	FABUS3	08	FABUS4	09	FABUS5	10	FABUS7	11	+5V
FR/W.H	12	TP102	TP123	13	FABUS0	TP103	14	FABUS2	TP104	15	FABUS1	TP105	16	DBUS7	TP106	17	CCASL	TP107	18	CROW0	TP108	19	CROW1	TP135
20	CRSEL.L	TP134	21	TP111	TP114	22	+5V	TP112	TP113	23	+5V	24	25	DBUS0	26	CSEL.L	27	MSIZE.H	28	DBUS6	29	DBUS4	30	DBUS5
31	PH2.H	32	DBUS3	33	DGND	34	CRAS.L	35	FABUS10	36	DBUS1	37	FABUS11	38	FABUS12	39	FABUS13	40	FABUS14	41	FABUS15	42	43	44

THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES
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DECIMALS .X ± ____ .XX ± ____ .XXX ± ____
ANGLES XX.X ± ____
FRACTIONS ± ____
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DRAWN BY Mike Collins DATE 11/11/85
CHECKED BY DATE
APPROVED BY DATE
RELEASED BY DATE

apple computer inc.

TITLE
UUT INTERFACE BOARD

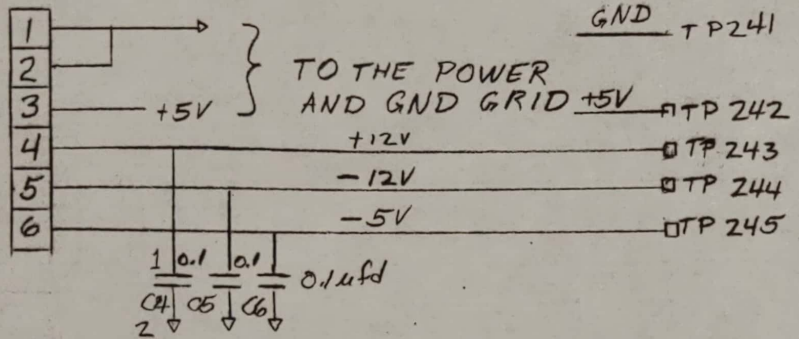
SIZE B
DRAWING NUMBER TSKA0013

MATERIAL:
FINISH:
SCALE:
SHEET 4 OF 6
NEXT ASSY.

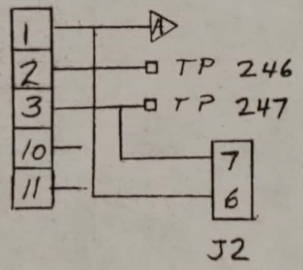
DRAWING NUMBER
SH OF

NOTE: UNLESS OTHERWISE SPECIFIED

J14 POWER CONNECTOR



J12 PHONE JACK



SLOT

IOSEL7	1	TP 248		23	TP 270		39	TP 286	
A0	2	TP 249		24	TP 271		40	TP 287	
A1	3	TP 250		25	TP 272		41	TP 289	
A2	4	TP 251		26	TP 273		42	TP 290	
A3	5	TP 252		27	TP 274		43	TP 291	
A4	6	TP 253		28	TP 275		44	TP 292	
A5	7	TP 254		29	TP 276		45	TP 293	
A6	8	TP 255		30	TP 277		46	TP 294	
A7	9	TP 256		31	TP 278		47	TP 295	
A8	10	TP 257		32	TP 279		48	TP 296	
A9	11	TP 258		33	TP 280		49	TP 297	
A10	12	TP 259		34	TP 281		50	TP 298	
A11	13	TP 260		35	TP 282				
A12	14	TP 261		36	TP 283				
A13	15	TP 262		37	TP 284				
A14	16	TP 263		38	TP 285				
A15	17	TP 264							
RW	18	TP 265							
SYNCL	19	TP 266							
IOSB	20	TP 267							
RDY	21	TP 268							
DMA	22	TP 269							

OUT1 OUT2 +5V DGND IN2 IN1 NMI IRQ RST INH -12V -5V CREF 7M Q3 PHI1

DEV0 DEV1 D7 D6 D5 D4 D3 D2 D1 D0 +12V

+5V

+12V

REV.	ZONE	ECO #	REVISION	APPD

ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
DECIMALS .X ± ____ .XX ± ____ .XXX ± ____
ANGLES XX.X ± ____
FRACTIONS ± ____
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.

DRAWN BY Mike Collins DATE 11/1/83
CHECKED BY DATE
APPROVED BY DATE
RELEASED BY DATE

apple computer inc.

TITLE: UUT INTER FACE BOARD

SIZE B | DRAWING NUMBER TSKA 0013

MATERIAL:

NEXT ASSY. | FINISH:

SCALE:

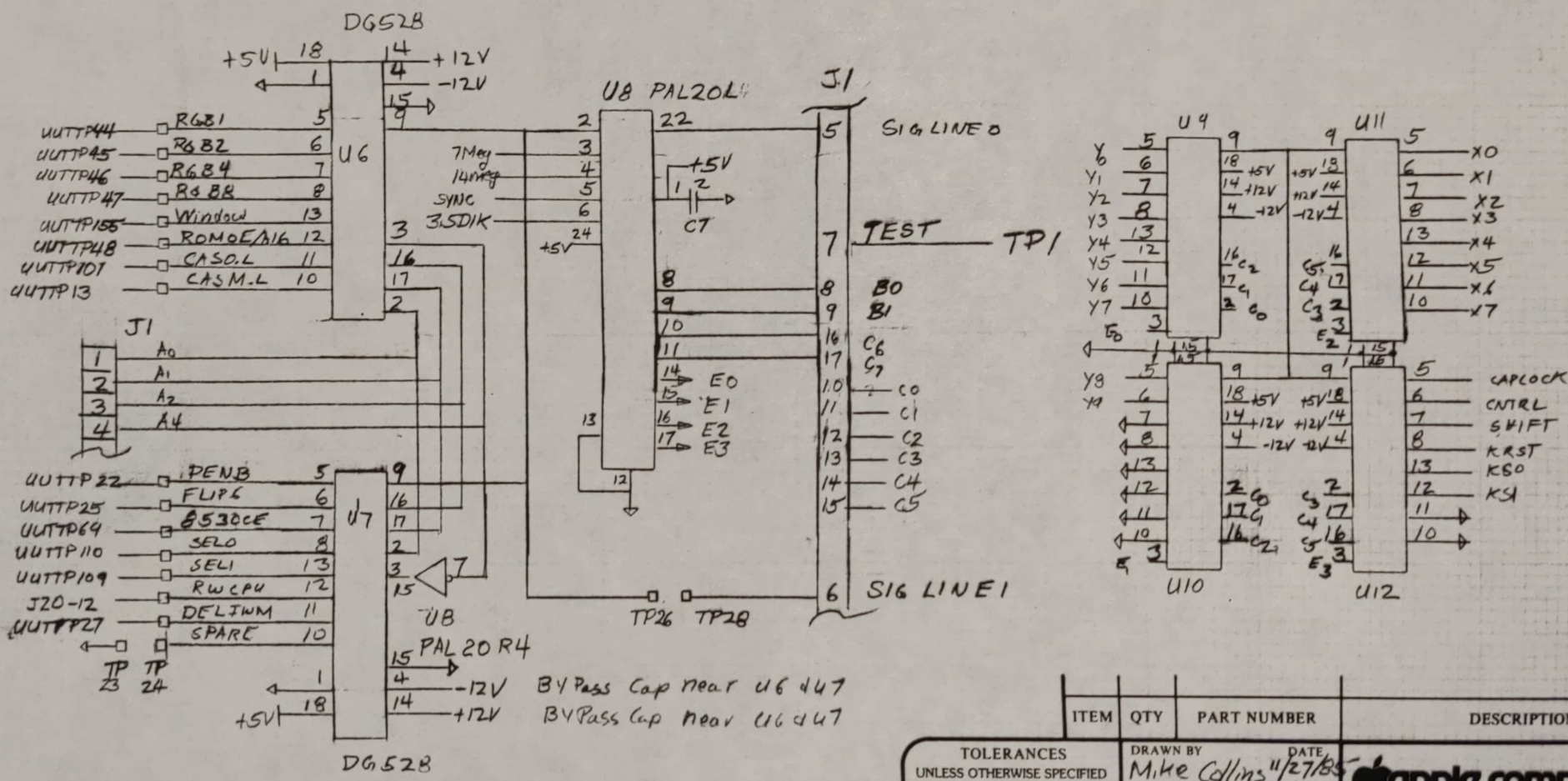
SHEET 5 OF 6

THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

DRAWING NUMBER | SH | OF

NOTE: UNLESS OTHERWISE SPECIFIED

REV.	ZONE	ECO #	REVISION	APPD
1		11/29	Add Signature Mux and J1	DWBC



ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES
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DECIMALS .X ± ____ .XX ± ____ .XXX ± ____
ANGLES XX.X ± ____
FRACTIONS ± ____
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DRAWN BY Mike Collins DATE 11/27/85
CHECKED BY DATE
APPROVED BY DATE
RELEASED BY DATE

apple computer inc.

TITLE
UUT INTERFACE Bd

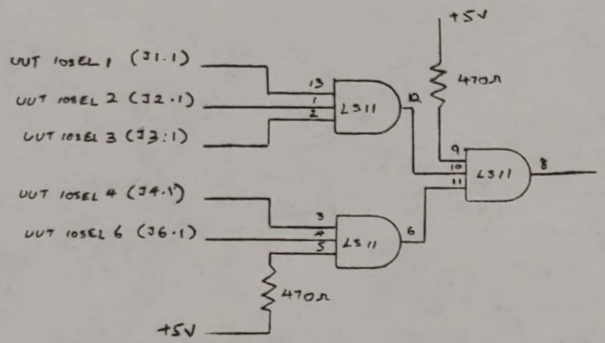
SIZE B
DRAWING NUMBER TSKA 0013

MATERIAL:
NEXT ASSY. FINISH:
SCALE:
SHEET 6 OF 6

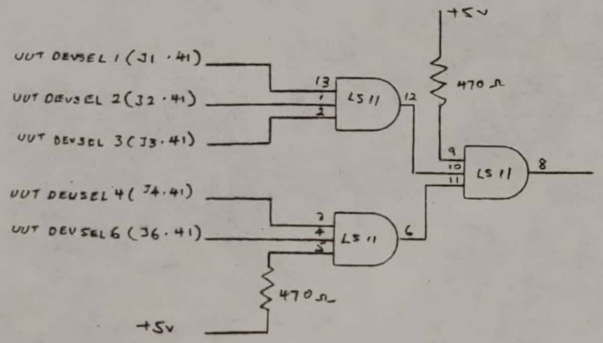
THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

NOTE: UNLESS OTHERWISE SPECIFIED

REV.	ZONE	ECO #	REVISION	APPD



To slot checker (slot 3) pin 1 (use wire-wrap)



To slot checker (slot 3) pin 41 (use wire-wrap)

7 - ⏚
14 - +5V (Vcc)

THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.
DECIMALS .X ± ____
.XX ± ____
.XXX ± ____
ANGLES XX.X ± ____
FRACTIONS ± ____
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.

DRAWN BY OON DATE 1/7/86
CHECKED BY DATE
APPROVED BY DATE
RELEASED BY DATE

apple computer inc.

TITLE: UUT INTERFACE BOARD

SIZE B
DRAWING NUMBER TSK A0013

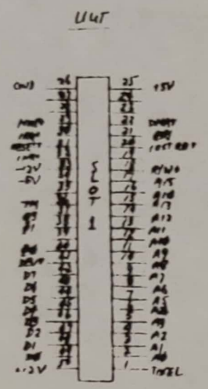
MATERIAL:
FINISH:
NEXT ASSY.
SCALE:
SHEET OF

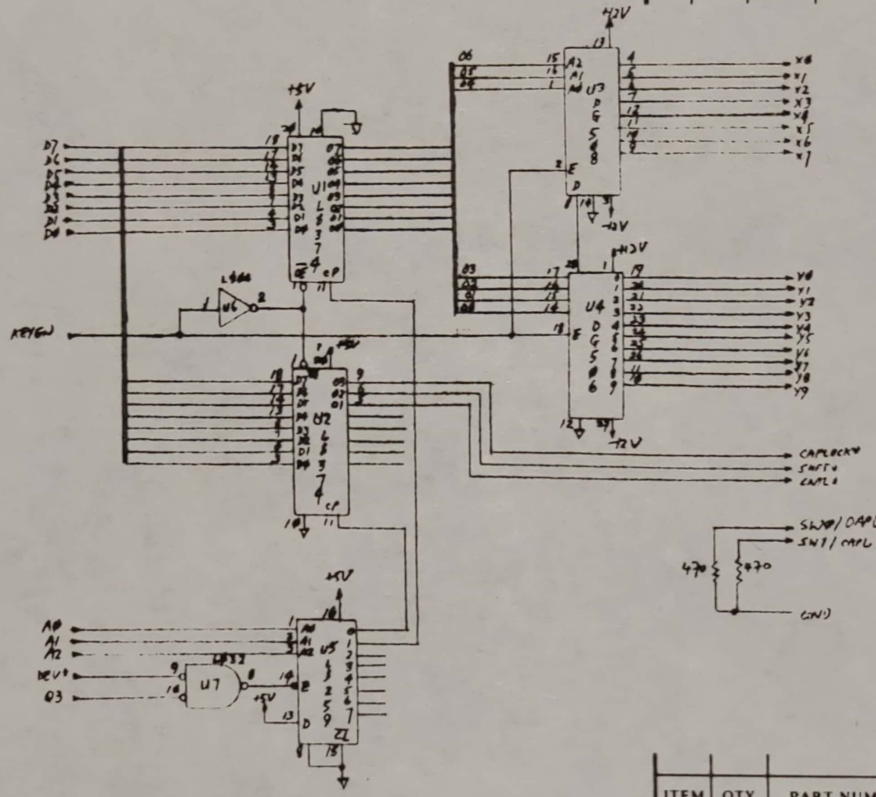
DRAWING NUMBER
SH OF

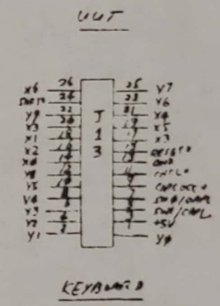
REV	ZONE	ECO #	REVISION	A

NOTE: UNLESS OTHERWISE SPECIFIED

1) ALL +5V TIED TO GND THRU .1μF CAP







	+5V	GND
LS32	14	7
LS04	14	7

ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
DECIMALS .X ± ____
.XX ± ____
.XXX ± ____
ANGLES XX.X ± ____
FRACTIONS ± ____
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS

DRAWN BY	DATE
K C Tan	1/8/86
CHECKED BY	DATE
APPROVED BY	DATE
RELEASED BY	DATE

apple computer

TITLE: ZEUS KEYBD EMULATOR

MATERIAL:

SIZE: B

DRAWING NUMBER: SYNG002-A

NEXT ASSY.

FINISH:

SCALE:

SHEET OF

THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

4 3 2 1

ADD TO U4T INTR

```
1 PAL20R4
2 U8 OF UUT INTFACE BOARD
3 DOES VARIOUS CONTROL FUNCTIONS
4 FOR KEYBOARD TEST AND SIGNATURE ANALYSIS
5 CLK SIG M7 M14 SYNC D3.5 A3 B0 B1 C6 C7 GND EN E0 E1 E2 NU17 NU18 NU19 NU
  20 E3 SIG DP VCC
6 DP = SIG*/M7*/B0*/B1+SIG*/M14*B0*/B1+SIG*/SYNC*/B0*B1+/SIG*/D3.5*B0*B1+DP
  *SIG
7 +DP*M7*/B0*/B1+DP*M14*B0*/B1+DP*SYNC*/B0*B1+DP*D3.5*B0*B1
8 SIG0= DP*M7*/B0*/B1+DP*M14*B0*/B1+DP*SYNC*/B0*B1+DP*D3.5*B0*B1+SIG0*DP
9 +SIG0= M7*/B0*/B1+SIG0*/M14*B0*/B1+SIG0*/SYNC*/B0*B1+SIG0*D3.5*B0*B1
10 E0 = C6
11 E1 = /C6
12 E2 = C6*C7 + /C6*/C7
13 E3 = /C6*C7 + C6*/C7
```


Mike Collins
1/3/86

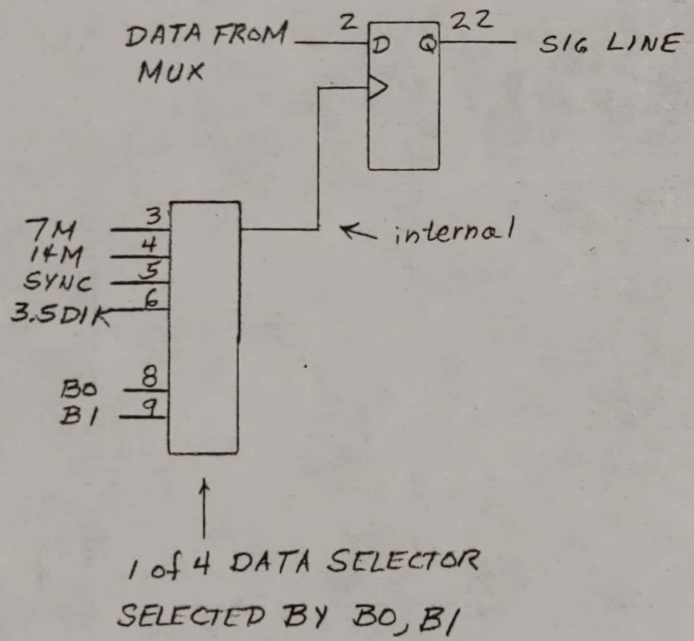
PAL EQUATIONS AND
LOGICAL EQUIVALENTS
UUT INTERFACE BD

TSKA 0028
PG1 OF 2

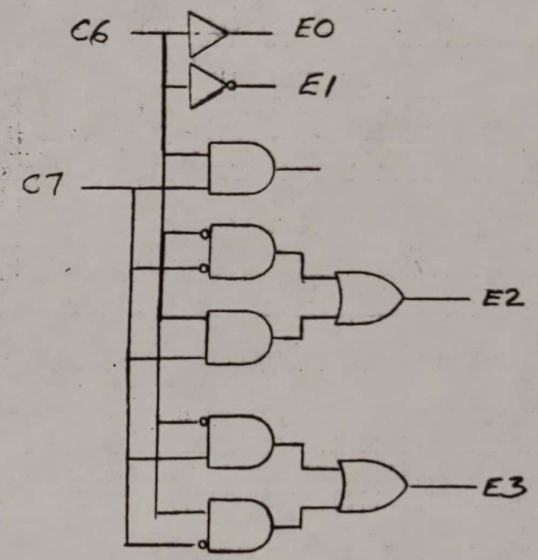
REV.	ZONE	ECO #	REVISION	APPD

NOTE: UNLESS OTHERWISE SPECIFIED

DATA SELECT FUNCTION



KEYBOARD MATRIX LOGIC
SELECTS MATRIX CONNECTION



DECODING

C7	C6	X	Y
0	0	U10 on	U11 on
0	1	U4 on	U12 on
1	0	U3 on	U13 on
1	1	U4	U11 on

A3 — 7 — 15

THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
DECIMALS .X ± ____ .XX ± ____ .XXX ± ____
ANGLES XX.X ± ____
FRACTIONS ± ____
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.

DRAWN BY Mike Collins DATE
CHECKED BY DATE 1/3/86
APPROVED BY DATE
RELEASED BY DATE

apple computer inc.

TITLE PAL EQUATIONS AND LOGICAL EQUIVALENTS

MATERIAL:
NEXT ASSY. FINISH:

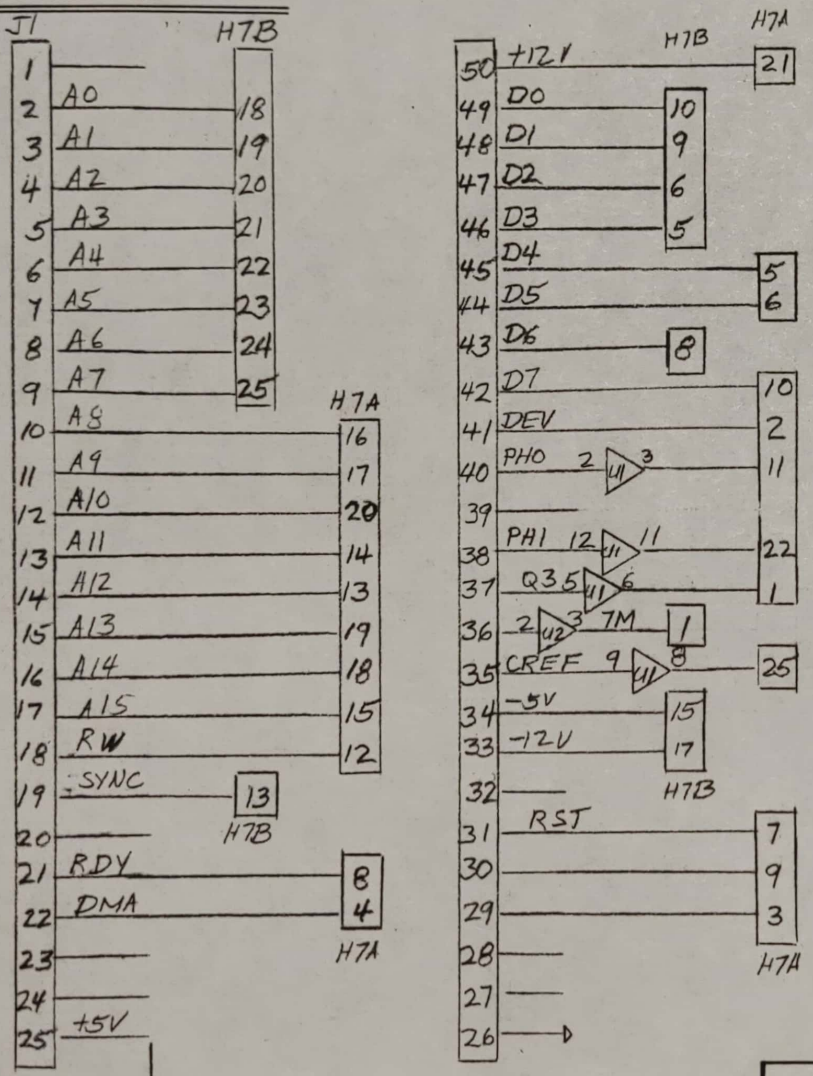
SIZE B
DRAWING NUMBER TSKA 0028
SCALE:
SHEET 2 OF 2

DRAWING NUMBER SH OF

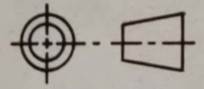

DMA PDL

J1 is Slot

NOTE: UNLESS OTHERWISE SPECIFIED



Pin 14 of 74LS125's



THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

REV.	ZONE	ECO #	REVISION	APPD

ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.
DECIMALS .X ± ____
.XX ± ____
.XXX ± ____
ANGLES XX.X ± ____
FRACTIONS ± ____
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.

DRAWN BY Mike Collins DATE 12/10/85
CHECKED BY DATE
APPROVED BY DATE
RELEASED BY DATE

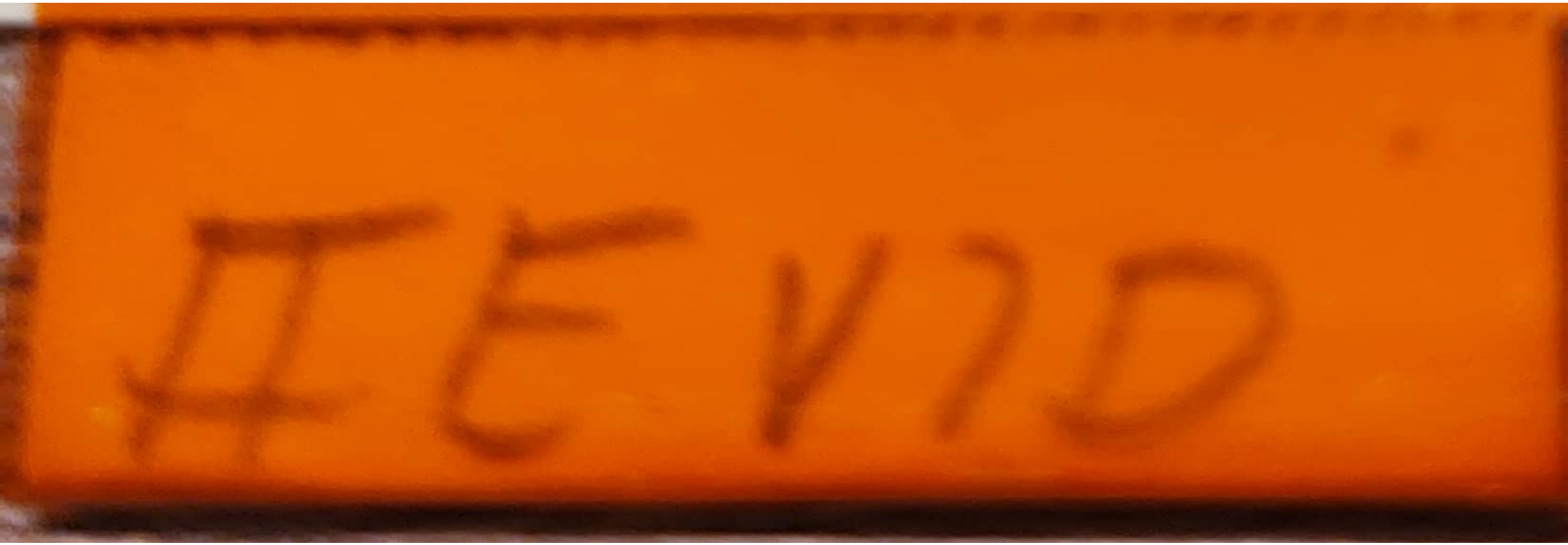
apple computer inc.

TITLE DMA Paddle Board Schematic

SIZE B
DRAWING NUMBER SKA 0020

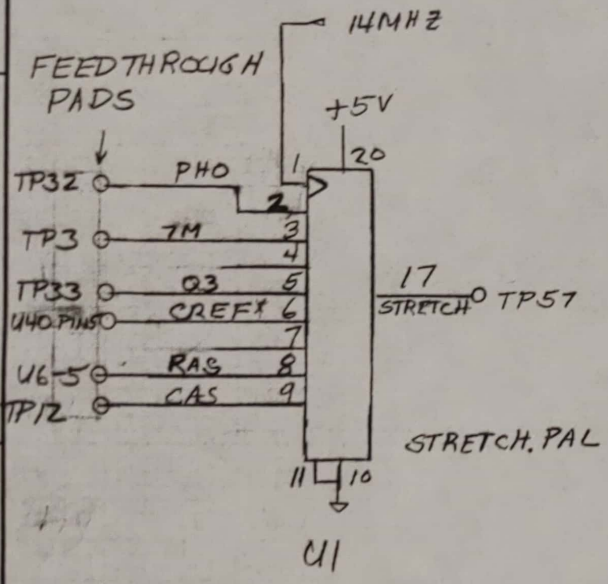
MATERIAL:
NEXT ASSY.
FINISH:
SCALE:
SHEET / OF /

DRAWING NUMBER
SH OF

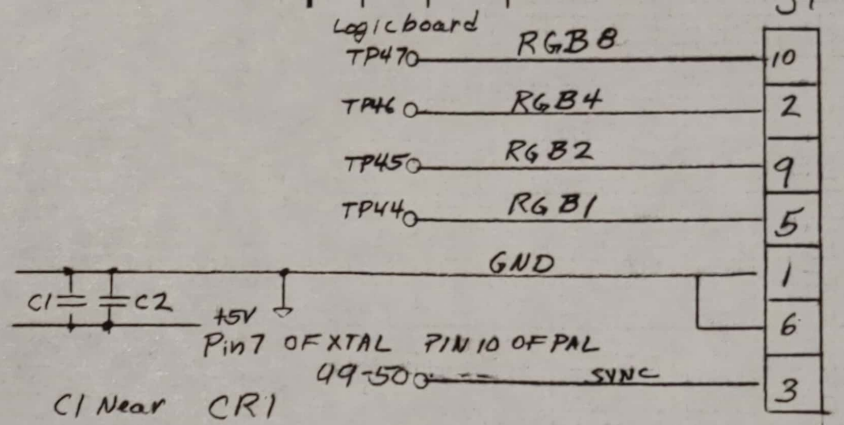

LEVID

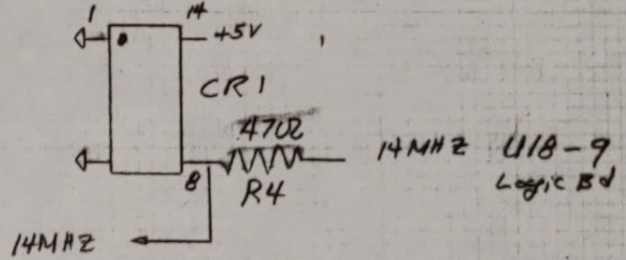
NOTE: UNLESS OTHERWISE SPECIFIED

REV.	ZONE	ECO #	REVISION	APPD



CREF is picked up on Top Side of the board





NOTE LOCATION OF Connections on Page2

ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.
DECIMALS .X ± ____
.XX ± ____
.XXX ± ____
ANGLES XX.X ± ____
FRACTIONS ± ____
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.

DRAWN BY Mike Collins DATE 12/20/85
CHECKED BY DATE
APPROVED BY DATE
RELEASED BY DATE

apple computer inc.

TITLE
Board To Add AIIE Video Without VGC

SIZE B
DRAWING NUMBER TSKA0014

MATERIAL:
FINISH:
NEXT ASSY.
SCALE:
SHEET 3 OF 3

THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

DRAWING NUMBER
SH OF

REV.	ZONE	ECO #	REVISION	APPD
1	Pg 1		Use PAL and OSCILLATOR	11/20/85

NOTE: UNLESS OTHERWISE SPECIFIED

AMP 747408

DB15

Side View

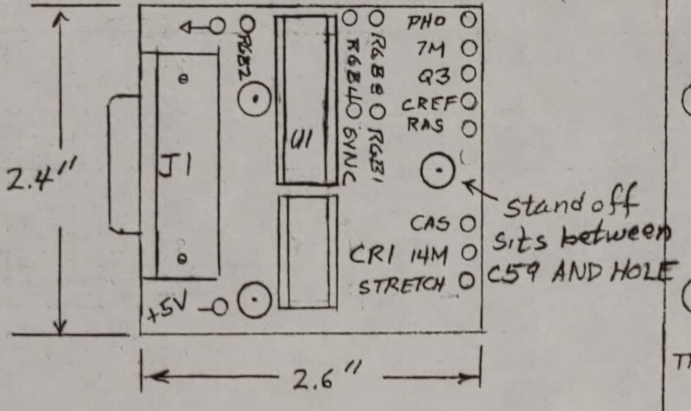
"Vector" Board

SOLDER GND HERE CALLED OUT AS "SHELL GND" on Schematic

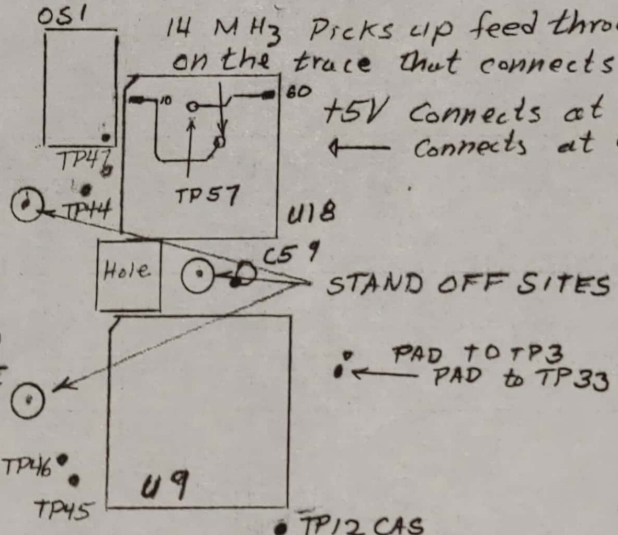
← Logic Board

↑ Wiring drops thru hole to back side of logic board

Approximately ½" standoff Gliptol or similar temporary glue can be used to hold board



stand off sits between C59 AND HOLE



Test points are vias with circles around them.

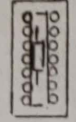
TP33 TP3 7M

TP32 PHO

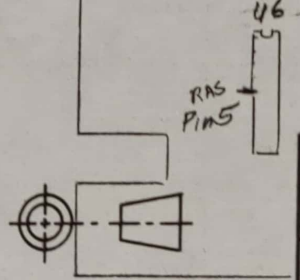
U40-25

Method Of adding 0.1 bypass to the IC socket

Top View



Axial lead 0.1uf cd in Cavity, Wire wrap leads to pins 7+14 Per schematic



THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
DECIMALS .X ± ___ .XX ± ___ .XXX ± ___
ANGLES XX.X ± ___
FRACTIONS ± ___
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.

DRAWN BY MB Collins DATE 11/14
CHECKED BY DATE
APPROVED BY DATE
RELEASED BY DATE

MATERIAL:
FINISH:
NEXT ASSY.

apple computer inc.

TITLE Assembly Board To Add AIIE Video Without VGC

SIZE B | DRAWING NUMBER TSK0014

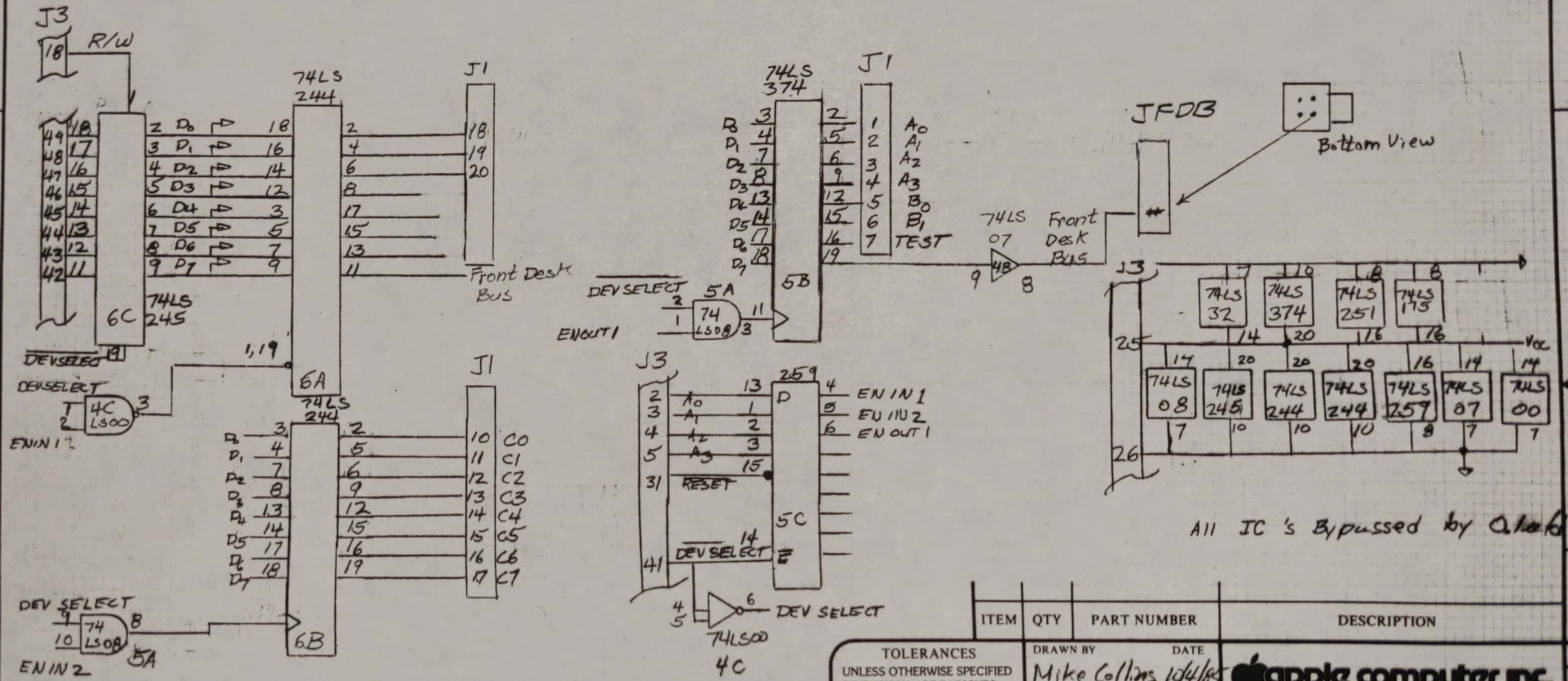
SCALE: | SHEET 2 OF 2


FDB1IWM

NOTE: UNLESS OTHERWISE SPECIFIED

J1 is 40 Pin edge connector
J2 is DB19 cable
J3 is card edge connector

REV.	ZONE	ECO #	REVISION	APPD
11/1			Added Ref Desig IWM Port tester	



ITEM	QTY	PART NUMBER	DESCRIPTION

TOLERANCES
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
DECIMALS .X ± ___ .XX ± ___ .XXX ± ___
ANGLES XX.X ± ___
FRACTIONS ± ___
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.

DRAWN BY Mike Collins DATE 10/4/85
CHECKED BY DATE
APPROVED BY DATE
RELEASED BY DATE

apple computer inc.

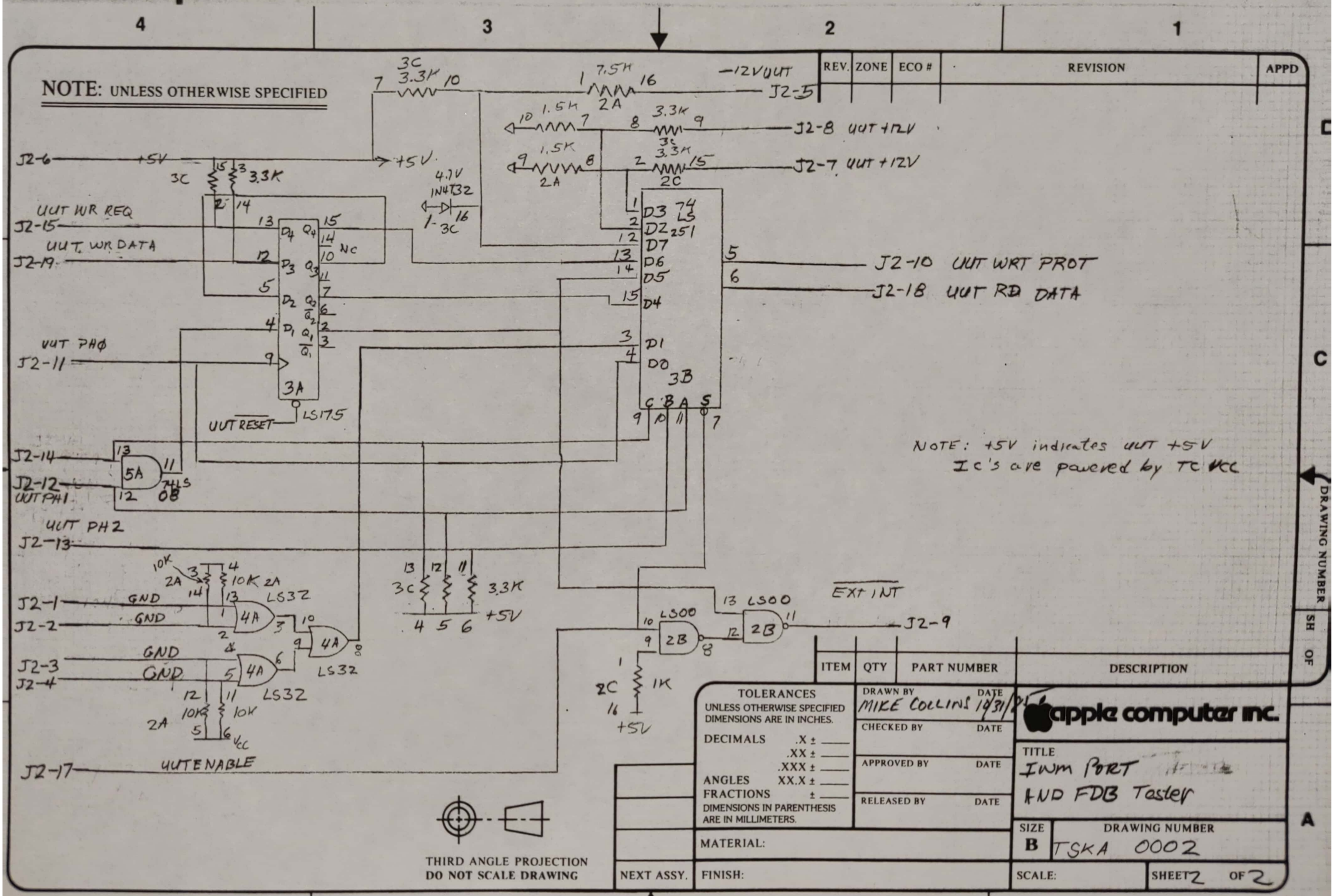
TITLE IWM PORT AND FDB TESTER

SIZE B | DRAWING NUMBER TSKA 0002

MATERIAL:
NEXT ASSY. | FINISH:
SCALE: | SHEET 1 OF 2

THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING

DRAWING NUMBER SH OF


NOTE: UNLESS OTHERWISE SPECIFIED
REV. | ZONE | ECO # | REVISION | APPD
-12V OUT
J2-5
J2-8 OUT +12V
J2-7 OUT +12V
J2-6 +5V
+5V
4.7V IN4732
UUT WR REQ
J2-15
UUT WR DATA
J2-19
UUT PHØ
J2-11
UUT RESET
LS175
J2-14
J2-12
UUT PH1
UUT PH2
J2-13
J2-1 GND
J2-2 GND
J2-3 GND
J2-4 GND
LS32
J2-17 UUTENABLE
74 LS 251
J2-10 UUT WRT PROT
J2-18 UUT RD DATA
NOTE: +5V indicates UUT +5V
IC's are powered by TC Vcc
EXT INT
LS00
J2-9
1K
+5V
ITEM | QTY | PART NUMBER | DESCRIPTION
TOLERANCES
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
DECIMALS .X ± .XX ± .XXX ±
ANGLES XX.X ±
FRACTIONS ±
DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.
DRAWN BY MIKE COLLINS DATE 10/31/81
CHECKED BY DATE
APPROVED BY DATE
RELEASED BY DATE
apple computer inc.
TITLE
IWM PORT AND FDB Tester
SIZE B
DRAWING NUMBER TSKA 0002
MATERIAL:
NEXT ASSY.
FINISH:
SCALE:
SHEET 2 OF 2
THIRD ANGLE PROJECTION
DO NOT SCALE DRAWING
DRAWING NUMBER
SH OF

To: KC Tan, Kari Grabe, Randy Carr

From: Mike Collins Jan 5, 1986

Subject: New Soft switches For IWM and FDB board.

The new board has a number of control lines that are used other places as well as the FDB port. There are 16 ouput lines and 8 input lines. There is a bank switching arrangement that allows us to select which group of 8 lines we want to access. To enable a bank we do an access to one of 3 even addresses. To disable that bank we do an access to the odd address above the even address.

The banks are assigned as follows:

Bank 0:

Bank 0 is enabled by accessing $C080 + slot number shifted left 4 places. To disenable simply access the next address above. Bank 0 is a byte of 8 inputs that can be read by reading any address assigned to this slot. There are 16 addresses assigned to each slot. If the programmer chooses to read from the first 6 addresses he will change the bank enable in some way. I suggest that reads be done from the bank number enabled.

Bank 0 currently only has one input assigned; this is the FDBus input path. This is in the D7 location of $C080 + slot#X16.

Bank 1:

Bank 1 resides at $C080 + slot#X16 +2.

This bank has 8 outputs. These are C0 thru C7 and are used only during board test to select a key for the keyboard test. The documentation for the UUT Interface board will explain how to use these lines. These lines go out thru the 40 pin connector to the UUT interface board.

Bank 2:

Bank 2 resides at $C080 + slot#X16 +4.

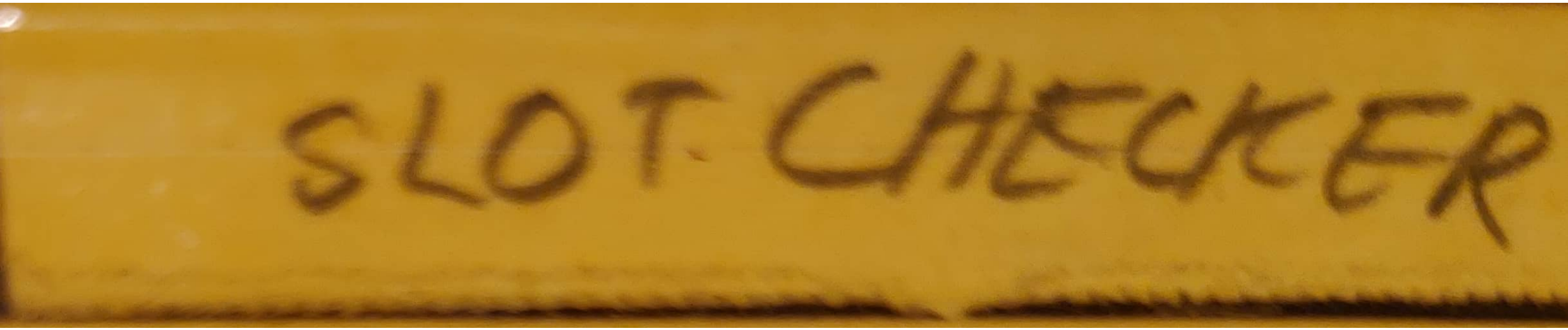
Bank 2 is another set of 8 outputs. The lines corresponding to D0 thru D3 are A0 thru A3. These are used by the UUT Interface board to select one of 16 signatures to be used by the signature tree on the UUT Interface board. This gives us an additional 16 points that we can access over the 24

already on the slot 7 signature control board. This allows the possible future growth into a more diagnostic oriented tester if necessary.

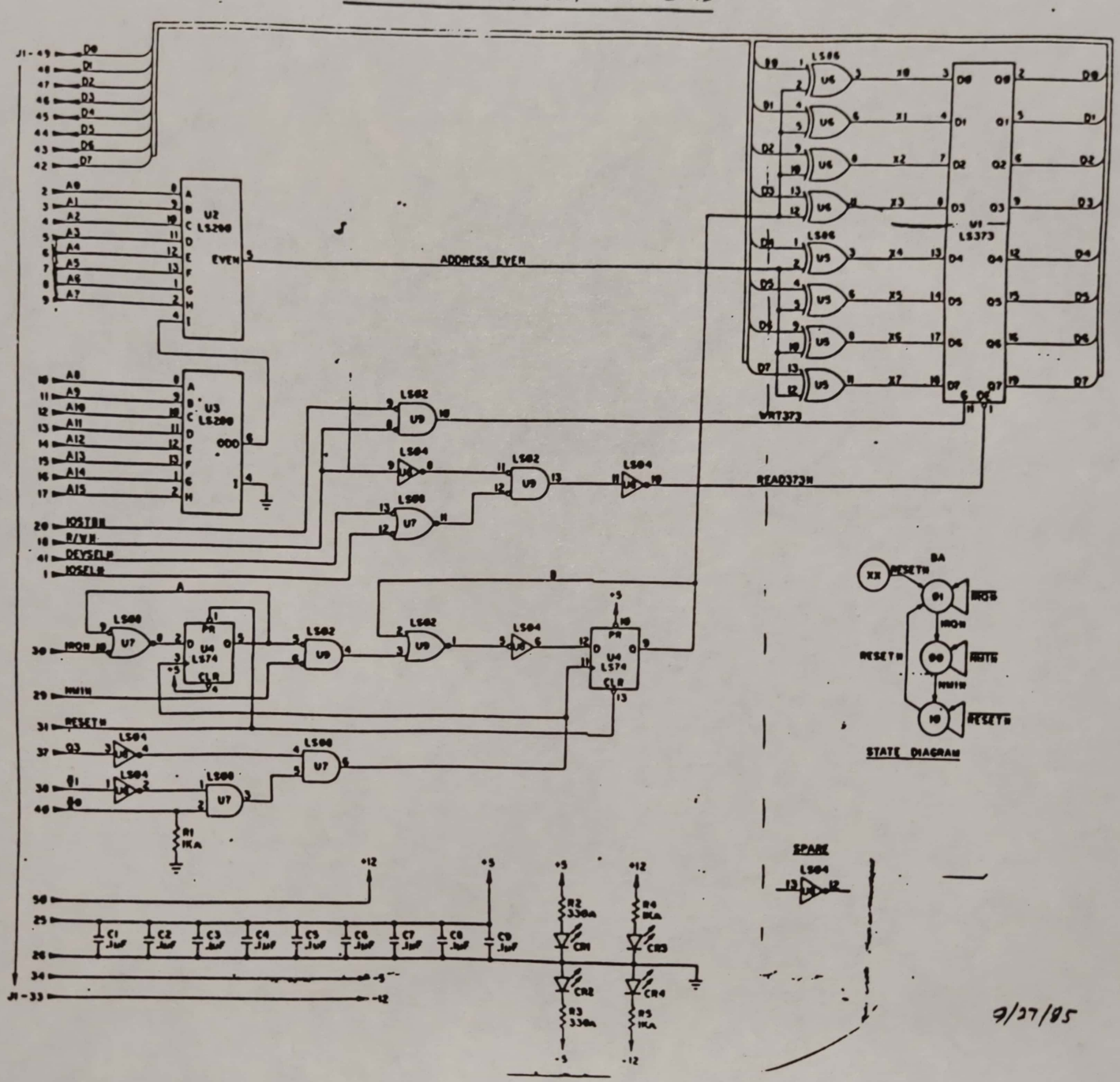
B0 and B1 are used by both the signature control board and the UUT Interface board to select one of 4 clocks for signature. The UUT interface board shifts the output of the signature tree through an edge triggered latch. This pipelining eliminates any concern about propagation time down the cable from the UUT to the test controller.

The Test output goes to the UUT Interface board to force the VGC into test mode.

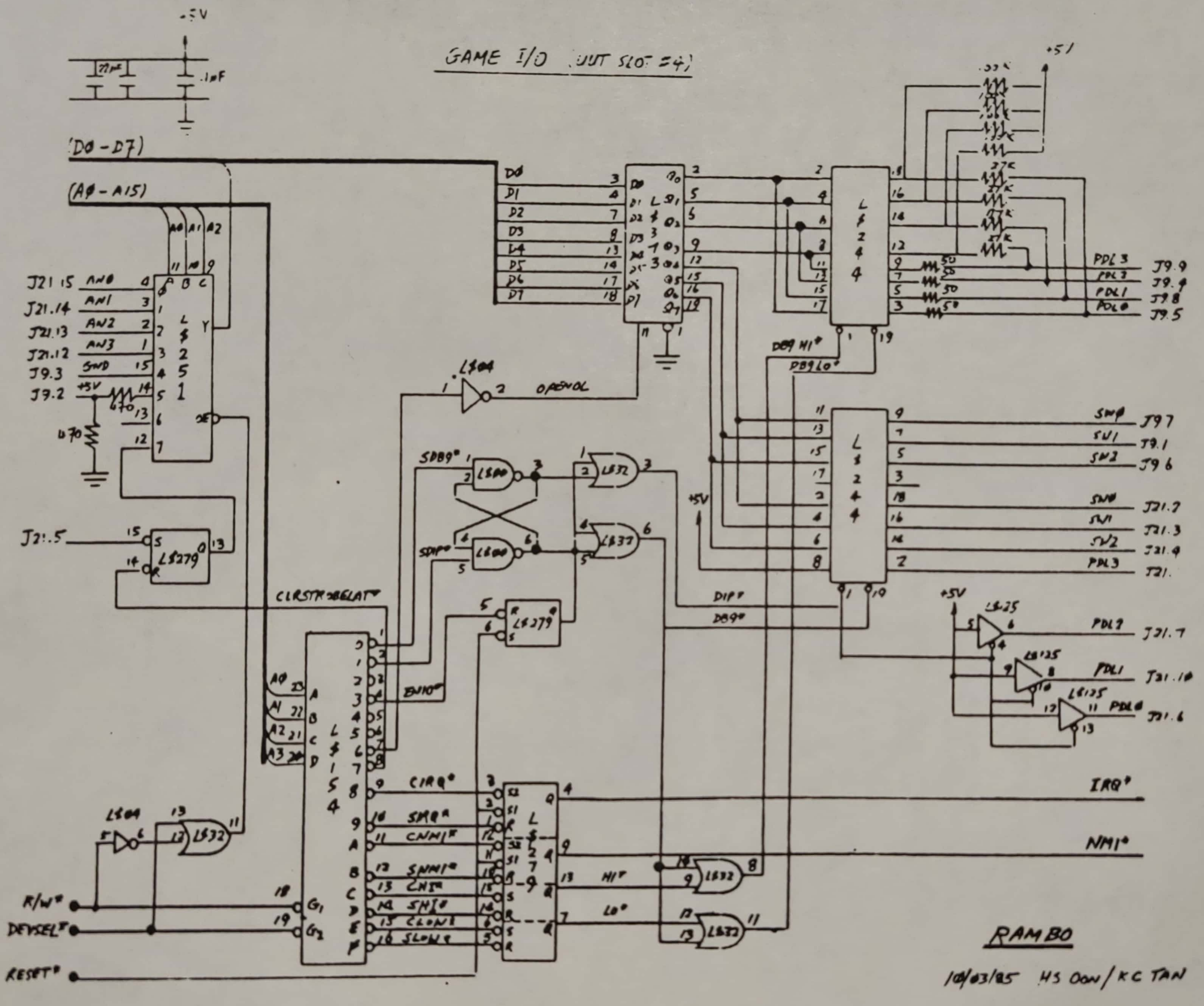
The last bit in the D7 position is the FDB output. This goes to an open collector device and out to the FDB.


SLOT CHECKER

UUT EXTERNAL I/O SLOT TEST CARD




GAME TJO


GAME I/O (OUT SLOT #4)
(D0 - D7)
(A0 - A15)
LS251
LS374
LS244
LS244
LS04
OPENOL
LS00
LS32
LS279
LS154
LS125
CLRSTROBELAT*
IRQ*
NMI*
R/W*
DEVSEL*
RESET*
RAMBO
10/03/85 HS Oon/KC TAN

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25071	BLACK
25072	LIGHT BLUE
25073	DARK BLUE
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25075	LIGHT GREEN
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25078	RED
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